ECG608 Fall 2020 Final Project:

A Switching Power Supply(SPS) Controller Chip for a Flyback SPS.

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1. Abstract

A switching power supply is a power supply that continuously switches between on and off states to avoid being in the high dissipation transitions, lessoning the energy wasted. A flyback converter is a buck-boost converter with the inductor split to form a transformer. When the switch is closed, the magnetic flux stores the energy. When the switch is opened, the magnetic flux drop, making the diode to forward-bias, and allow current to flow from the transformer and charges the capacitor and the load. The chip designed for the project takes in a 5V source divided from the outlet, generates a constant 1.25V to compare with the voltage of the load. If the load is low on voltage, the chip charges with the frequency of 5MHz. If the load is high, the chip does not charge.

2. Theory of operation

The scope of the project is to design a reference chip for the flyback SPS. The chip consists of 4 simple main components: a bandgap, a comparator, an oscillator, and a buffer.

First, a bandgap outputs a reference voltage. The intent of the device is to keep the load charged at 12.5V. The bandgap that outputs a constant 12.5V will be power consuming. The 1pF capacitor is there to reduce the ripple and noise. The device uses the 10-to-1 voltage divider that are made of hi-res poly resistors to divide the input load voltage. The bandgap then outputs a constant 12.5V reference voltage to be compared.

Second, the comparator compares the output from the bandgap and the divided input voltage. It outputs a 5V when the bandgap output is higher than the divided input voltage and outputs a 0V vice versa.

Third, the oscillator outputs 5V with the frequency of 5MHz and the rise and fall time of 1ns only when the output of the comparator is 0. Other times, it will output a 5V to be later inverted with the buffer. This is due to the NAND2 gate. The truth table of the NAND2 gate is under the NAND2 gate part of the paper.

Lastly, the buffer simply boosts the current of the output of the oscillator as well as to invert it. It draws current from the VDD and adds it to the signal.

3. Datasheet

DC Voltage	5V
Current Range	10mA-2.5A
Rated Power	0.64W
Ripple Voltage	190mV
Voltage Adj. Range	4-5V
Rise/fall time	1ns
Frequency range	75kHz-5.7MHz
Efficiency	97.98%
Working temp.	0 – 100℃

Rated power is calculated as the input voltage times the input current.

Ripple & noise is interpreted from the maximum ripple voltage.

Current range was interpreted based on the efficiency. 10mA minimum was taken because the efficiency will go below 80% if the load current is lower than that.

Ripple voltage was taken as the maximum ripple voltage at 5V.

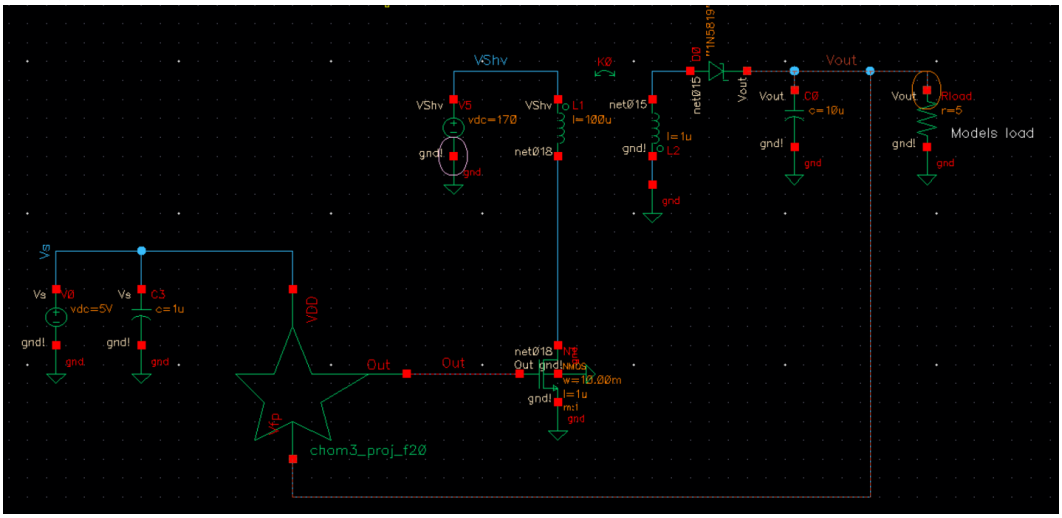
Voltage Adj. Range is the range over which the output voltage can be varied and still maintain the desired voltage of 5V.

Frequency range was determined by the variable load current range.

The efficiency was determined by the maximum efficiency under 5V VDD and 27℃.

The working temperature was determined by the testing temperature range, as all the temperature points tested were fairly optimal.

4. Top file schematic, layout, and results



Off-chip board Schematic

The 170V is the voltage source from the power outlet, which is roughly 120 times the square root of 2. The 5V is split from the power source and powers the chip. The load in the figure is set to 5Ω but it can vary, and the varying load performance can be found in the report later. The scope of the project is to design the chip shown as "chom3_proj_f20."

The design symbol(the star) has the same footprint as the ideal symbol footprint so that it can be tested rapidly.

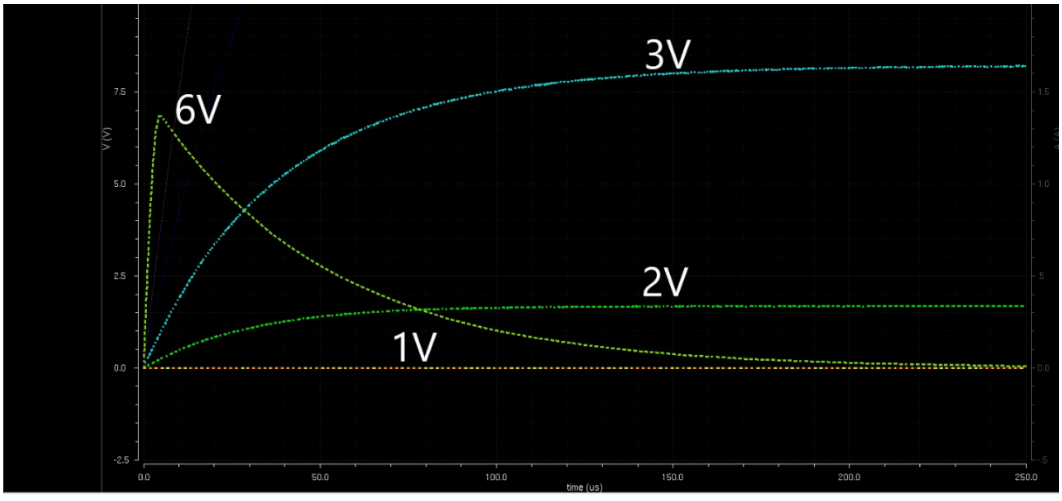
I have performed 3 different parametric analysis on the device. The first is the VDD input voltage, the second is load current, and the third is temperature sweep. Because each analysis were single variable analysis, other factors can be interpreted interchangeably (ex. You might expect the temperature vs efficiency relationship will also apply to the 3V VDD setup even though it was not proven by the simulation).

4.1. VDD parametric analysis

VDD dependence measurement at 27°C with a load of 5Ω							
VDD (V)	Minimum Voltage (V)	Maximum Voltage (V)	Ripple Voltage (V)	Frequency (Hz)	Input Power (W)	Output power (W)	Efficiency (%)
0	0			0	1.7p	0	N.A.
1	91.05n		<1m	34k	2.66μ	565.42a	>0
2	1.49		<1m	1.28M	8.58	443.4m	5.17
3	6.91		<1m	2.62M	32.64	9.55	29.26
4	12.83	13.24	205m	3.85M	37.26	33.64	90.28
5	12.31	12.69	190m	5.71M	31.66	31.02	97.98
6	1.45V		<1mV	0	1.00m	420.9m	N.A

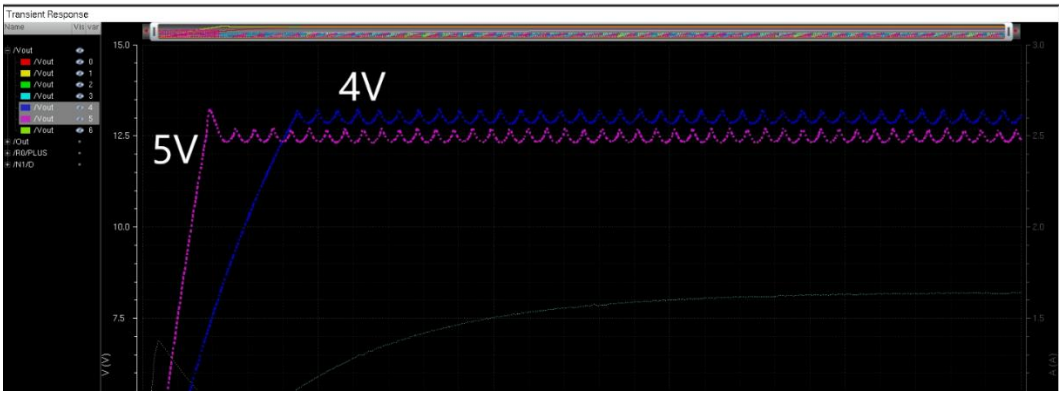
The above data shows that as the input VDD increases the efficiency increases. It can also be noted that the device is not functional at the voltage lower than 3V and higher than 6V. This also shows that even though the device will function with the 4V source, but it will have a significant reduction in the frequency as a drawback. This also increases the ripple voltage.

The input power was calculated by multiplying the average current through the big CMOS and through the 5V voltage source that powers the chip by 170+5V. The output power was calculated by multiplying the average load current by the average load voltage. This can also be done in many different ways such as current square times the resistance.



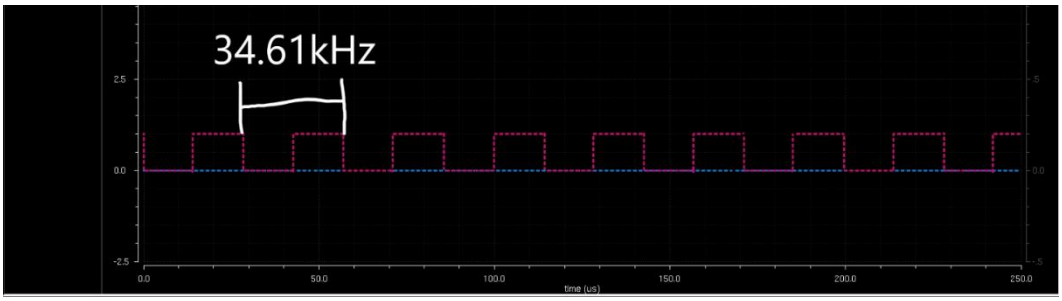
VDD transient analysis (Vout @ 0-3V & 6V) at 27°C with a load of 5Ω

The first test performed was the VDD parametric transient analysis from 0V to 6V. The result above shows that the device does not perform as desired from 0-3V VDD. Interestingly, the device also does not perform well with overvoltage of 6V. The desired result of the chip is to have the load voltage oscillate close to 12.5V. With too little or too much VDD, the device fails to charge. The possible reason for the 6V VDD failure might be explained by the result that the output voltage of the comparator was directly related to the VDD input, and the VDD input of 6V will cause the comparator to output a 6V output.

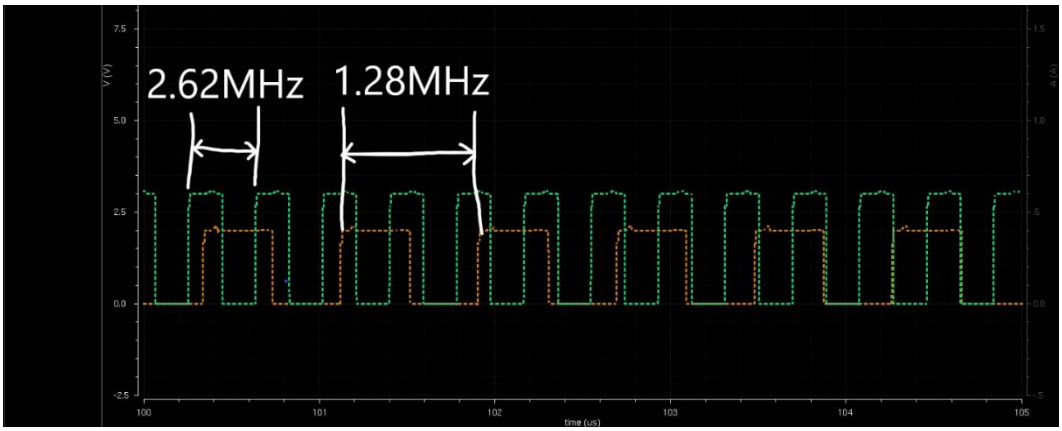


VDD transient analysis (Vout @ 4V & 5V) at 27℃ with a load of 5Ω

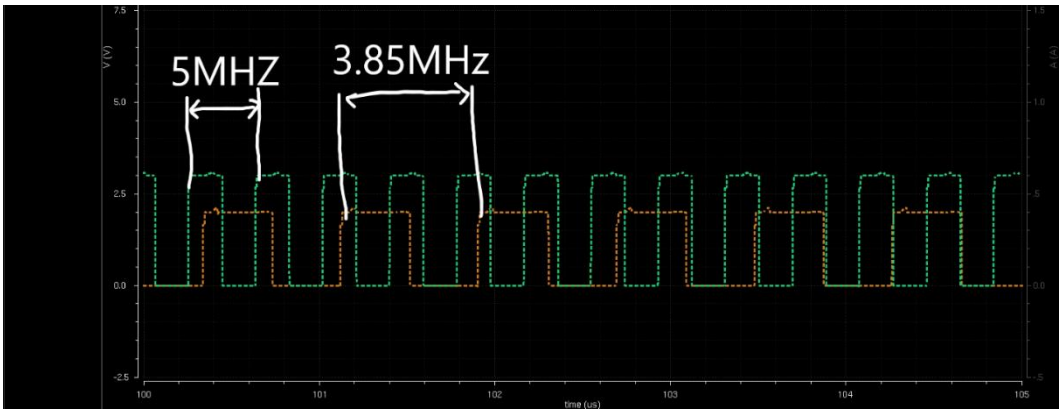
As the reader can see from the result above, the chip functions as desired within the range of 4-5V of VDD. However, we can see that the 4V VDD outputs slightly higher mean voltage to the load. This is due to the result that the comparator will only output 4V when the VDD is 4V. This leads to the oscillator reaching the 5V high but not quite reaching down to 0V. This problem can be fixed with the future work to make the comparator output a 5V with the 4V VDD input as well as to improve the oscillator to function optimally at 4V VDD.



VDD transient analysis (Out @ 0, 1V) at 27℃ with a load of 5Ω



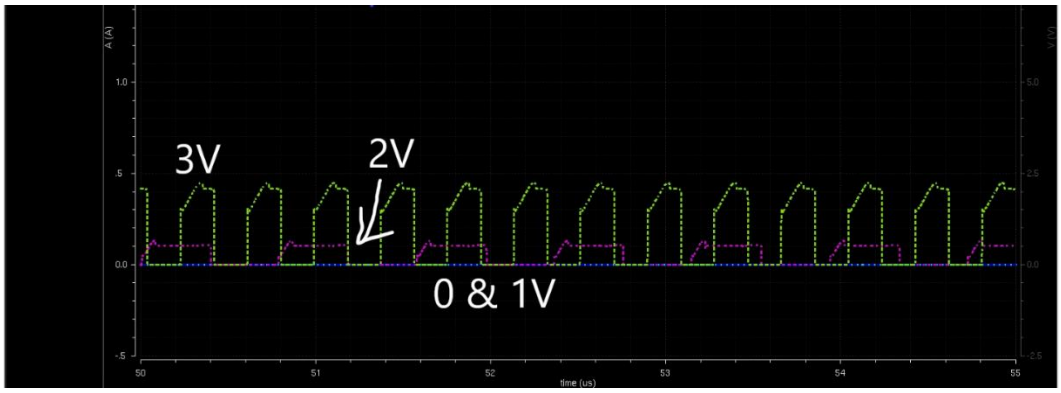
VDD transient analysis (Out @ 2, 3V) at 27℃ with a load of 5Ω



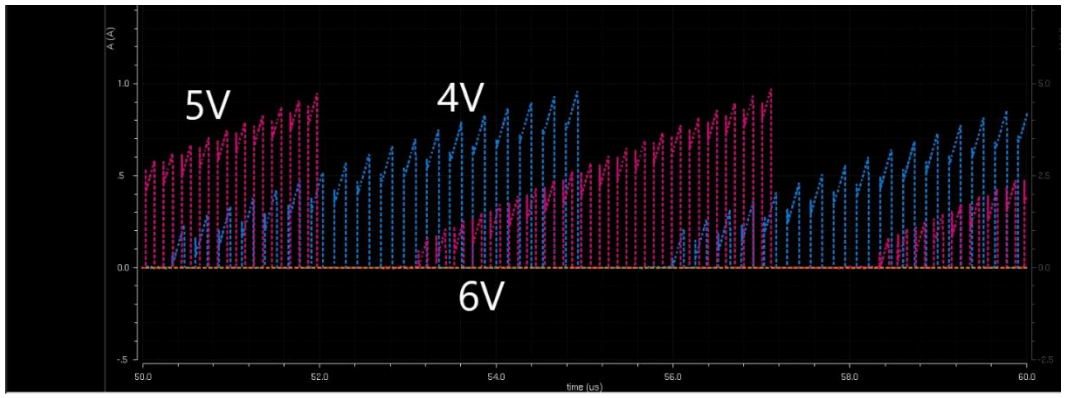
VDD transient analysis (Out @ 4, 5V) at 27℃ with a load of 5Ω

The frequencies at 0 to 4V VDD does not output the desired frequency of 5MHz. This is because as the VDD goes down below 5V, the oscillator is not capable of

oscillating at such a high frequency. For the future work, a modification to the oscillator to work with a 4V VDD better than 3.85MHz frequency would improve the stability and efficiency of the chip.

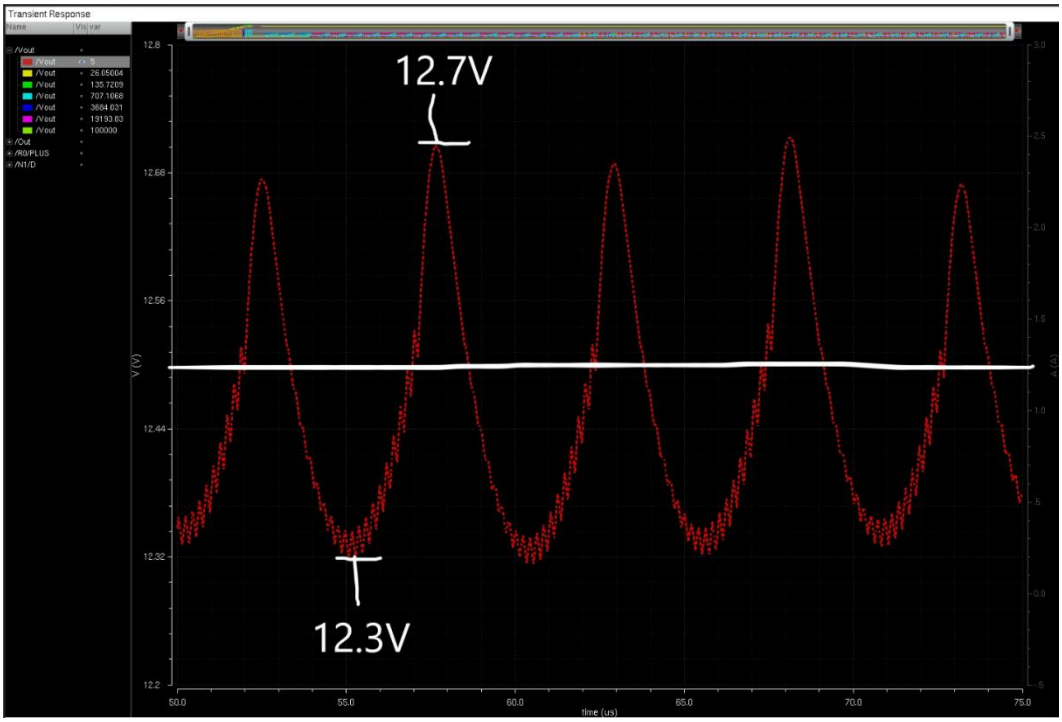


VDD transient analysis (I_{input} @ 0-3V) at 27°C with a load of 5Ω



VDD transient analysis (I_{input} @ 4-6V) at 27°C with a load of 5Ω

The input current determines the input power and charges the load by activating the transformer whenever the switch (the big NMOS) is opened. The current spikes represent the time when it opens. Then the gradual increase in the current represents the charging period of the transformer. The 6V VDD input will always have the big CMOS open, preventing it to have any current. This explains the zero-input current shown above.



Ripple voltage at temperature of 27℃ with a load of 5Ω

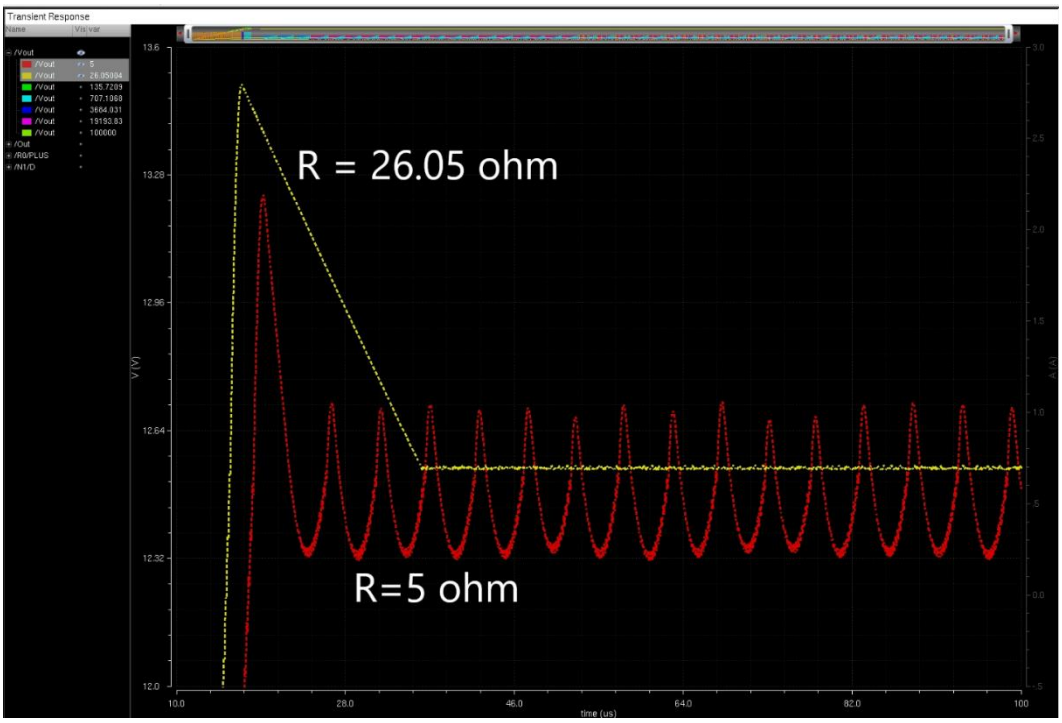
The above graph shows the ripple voltage at the ideal condition. However, as the load current testing shows below, the ripple voltage will decrease as the load current gets smaller. To decrease the ripple voltage for the higher load current, adding additional inverters in the chip to make the switching behavior faster. However, the drawback of this design is that it will consume more power than usual. However, by looking at the efficiency, the chip can take some percentage decrease. Another way to reduce the ripple is to decrease the length of the long L NMOSes used in the chip to make it faster, but it has its own drawback that it will not be able to handle higher voltages as well.

4.2. Load current parametric analysis

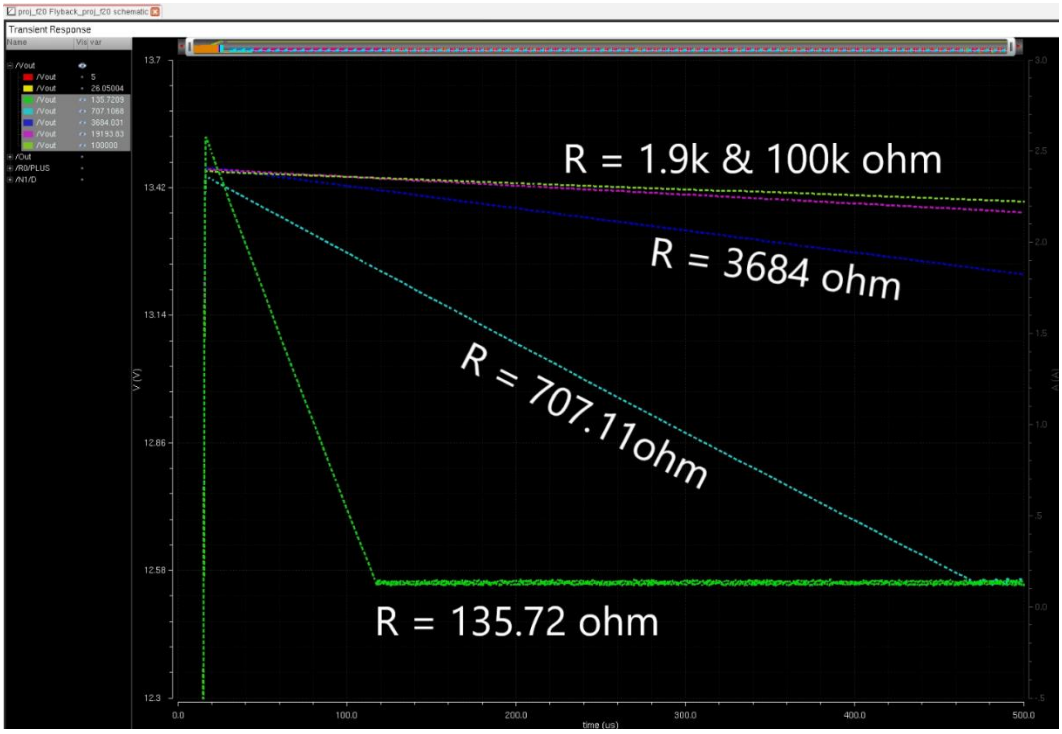
Load resistance to load current conversion									
Load resistance (Ω)	5	6.28	12.53	26.05	62.59	135.72	1.25k	3.69k	99.5k
Load current (A)	2.5	1.99	997.7m	479.9m	199.7m	92.10m	10.04m	3.39m	125.6μ

Load Current dependence measurement at temperature of 27°C							
Load Current (A)	Minimum Voltage (V)	Maximum voltage (V)	Ripple Voltage (V)	Frequency (Hz)	Input Power (W)	Output Power (W)	Efficiency
2.5	12.31	12.69	190m	5.71M	31.66	31.02	97.98%
1.99	12.34	12.58	120m	5.71M	25.83	24.73	95.74%
997.7m	12.45	12.50	25m	5.70M	13.14	12.44	94.67%
479.9m	12.54		<1m	3.57M	6.28	6.04	96.18%
199.7m	12.48		<1m	2.35M	2.62	2.49	95.04%
92.10m	12.55		<1m	756.8k	1.22	1.16	95.08%
10.04m	12.55		<1m	74.97k	143.7m	126.m	87.68%
3.39m	12.56		<1m	32.94k	81.1m	47.68m	58.79%
125.6μ	12.56		<1m	8.29k	18.5m	1.58m	8.54%

The above data shows that as the load current goes down the ripple voltage goes down. It can also be noted that the frequency will go down as the load current. This trend is evident in the power consumption and the efficiency as well. This goes to say that the clear drawback of the chip is that it will not be able to handle bigger load resistance with a desirable efficiency, but it will have a little ripple.

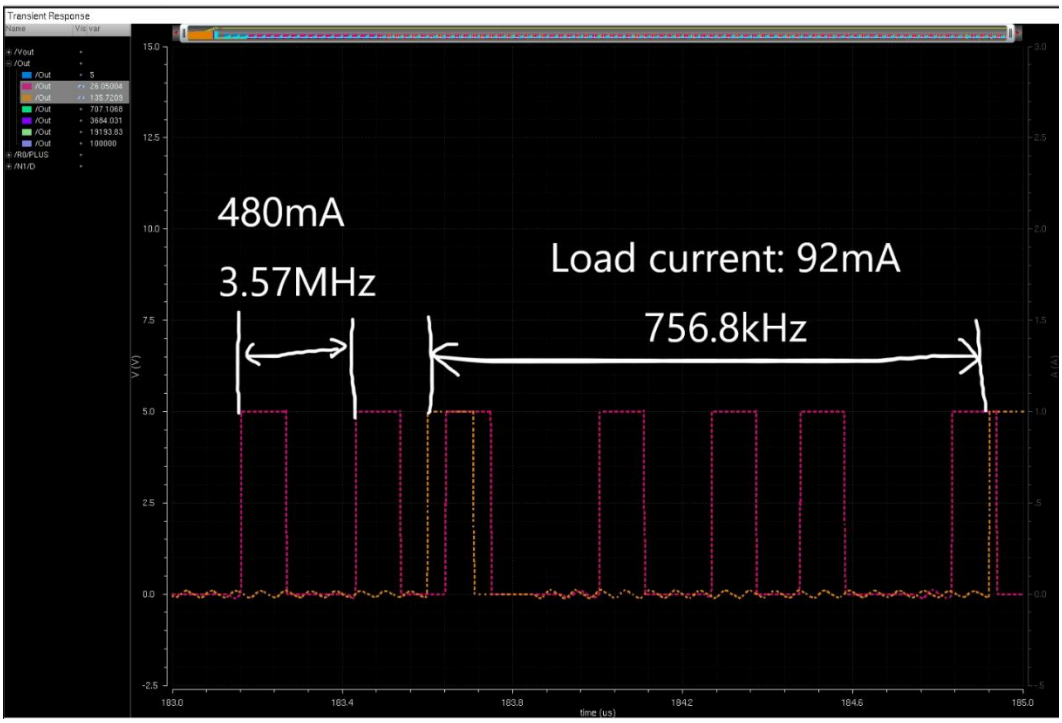


Load resistance transient analysis (Vout @ 5 & 26.05Ω) at 27℃



Load resistance transient analysis (Vout @ 135.72 – 100kΩ) at 27℃

As you can see from the graphs above, the increase in load resistance is directly correlated to the ripple voltage and the time it takes to stabilize. Higher loads cannot stabilize within 500μs time period of the simulation. This determines the acceptable operating input current and resistance range of the device.



Load resistance transient analysis (Out @ 26.05 – 135.7Ω) at 27℃

The above graph highlights the positive correlation between the load current and the oscillation period. The oscillation will be decreased because there is a bigger load to drive.

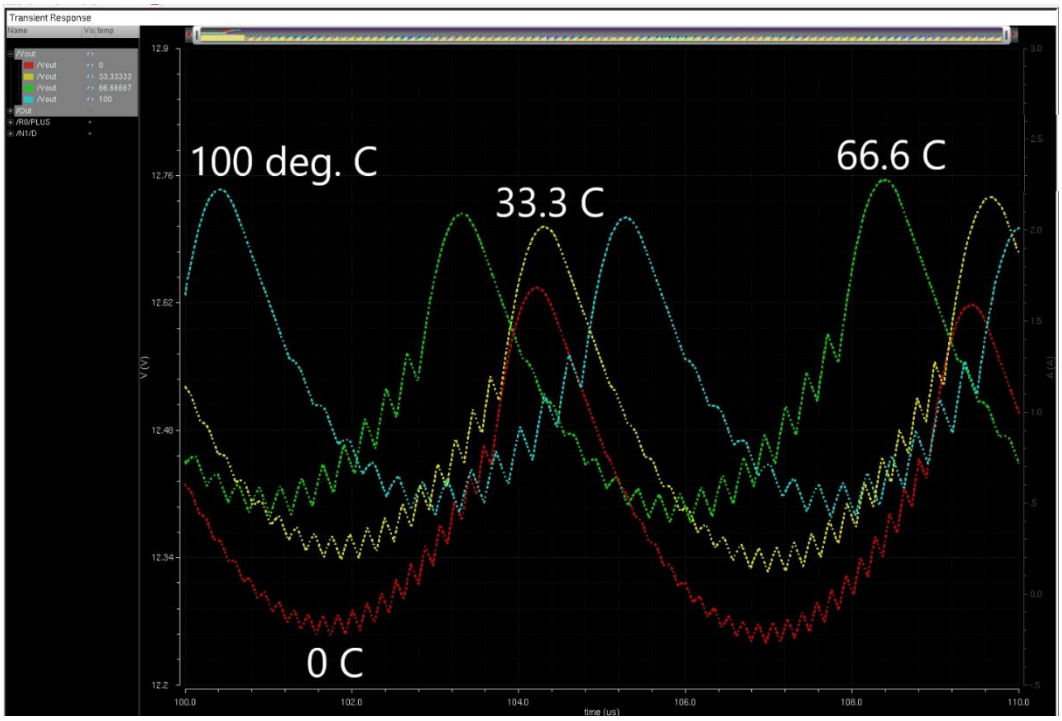
4.3. Temperature parametric analysis

Temperature dependence measurement with the load resistance of 5Ω at 5V VDD							
Temperature	Minimum Voltage	Maximum Voltage	Ripple Voltage	Frequency	Input Power	Output Power	Efficiency
0℃	12.25V	12.67V	210mV	5.71MHz	33.01 W	30.72 W	93.06%
27℃	12.31V	12.69V	190mV	5.71MHz	31.66 W	31.02 W	97.98%
33.3℃	12.32V	12.72V	200mV	4.74MHz	33.56 W	31.58 W	94.10%
66.6℃	12.39V	12.75V	180mV	3.96MHz	33.41 W	31.82 W	95.24%
100℃	12.38V	12.77V	195mV	3.43MHz	33.52 W	31.32 W	93.44%

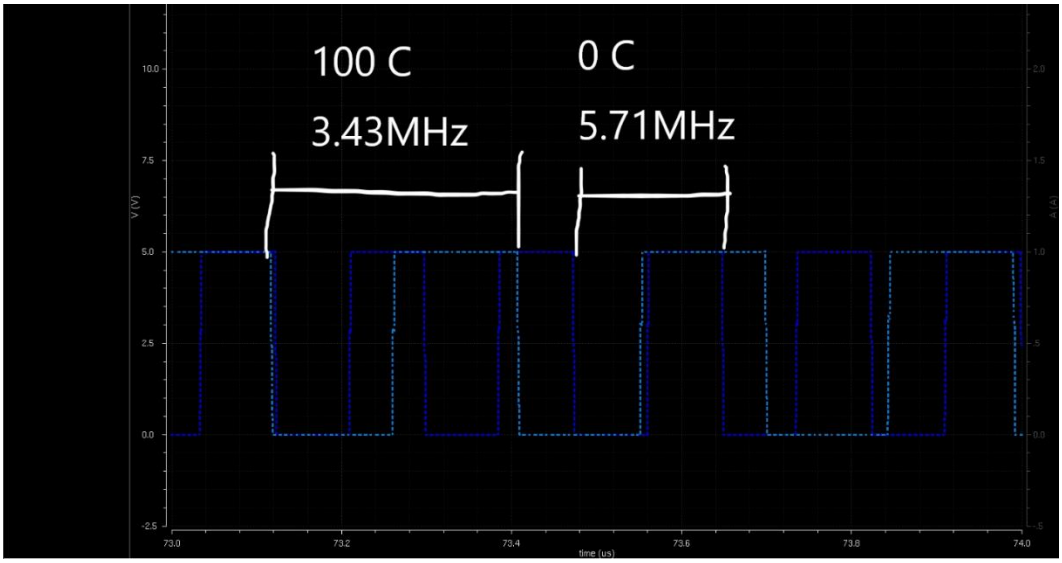
From the data above, it can be shown that the higher temperature drives the output voltage up. However, it did not alter the ripple voltage significantly. It did show that there is a negative relationship between the temperature and the frequency of the output. Although the efficiency showed the decreasing trend, strangely, the 0℃ efficiency was the outlier of this trend. It would make sense to have the efficiency driven down by the temperature because the further analysis of the individual components shows that their power consumption went up with the temperature. This temperature dependence can be explained by the body effect equation,

$$\emptyset_F = (\frac{kT}{q})ln(\frac{N_A}{n_i})$$

Where $\emptyset_F$ is half the contact potential, k is Boltzmann's constant, T is temperature, q is the elementary charge, N_A is a doping parameter and n_i is the intrinsic doping parameter. This means that the threshold voltage will increase as the temperature increases.

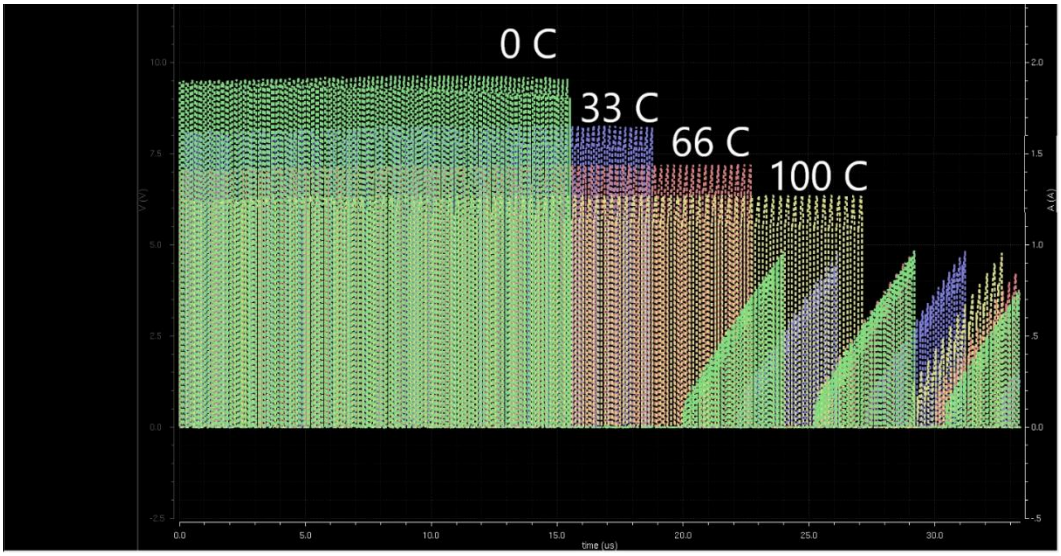


Temperature transient analysis (Vout) with the load resistance of 5 Ω at 5V VDD



Temperature transient analysis (Out @ 0 vs 100℃) with the load of 5 Ω at 5V VDD

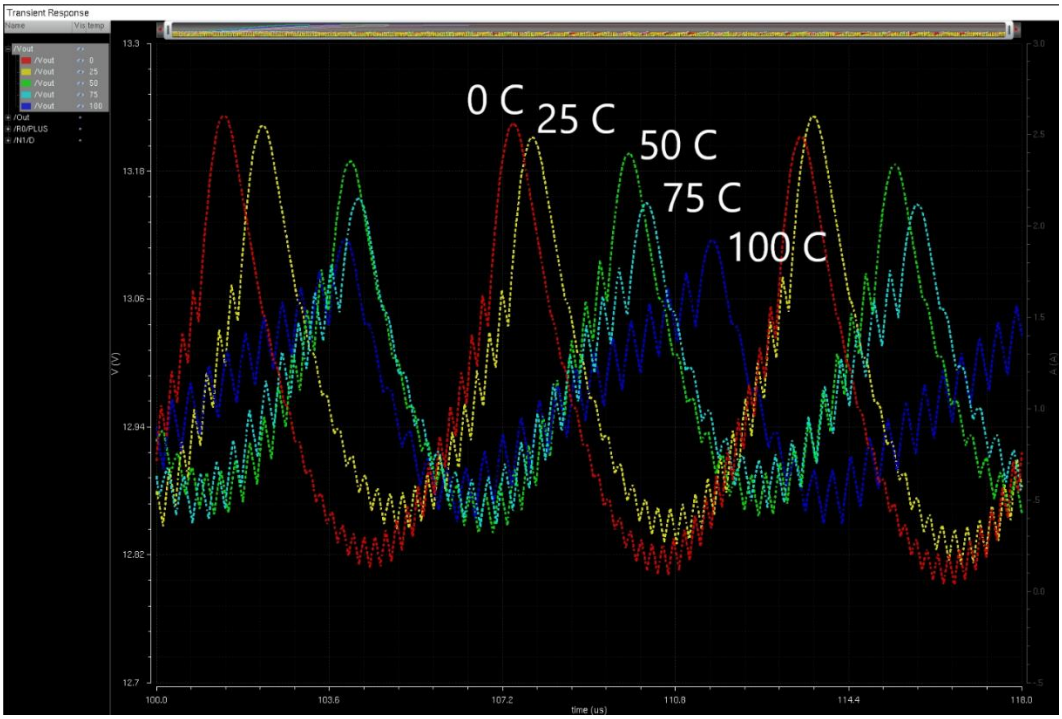
The above graph shows the negative relationship with the frequency of the output and temperature.



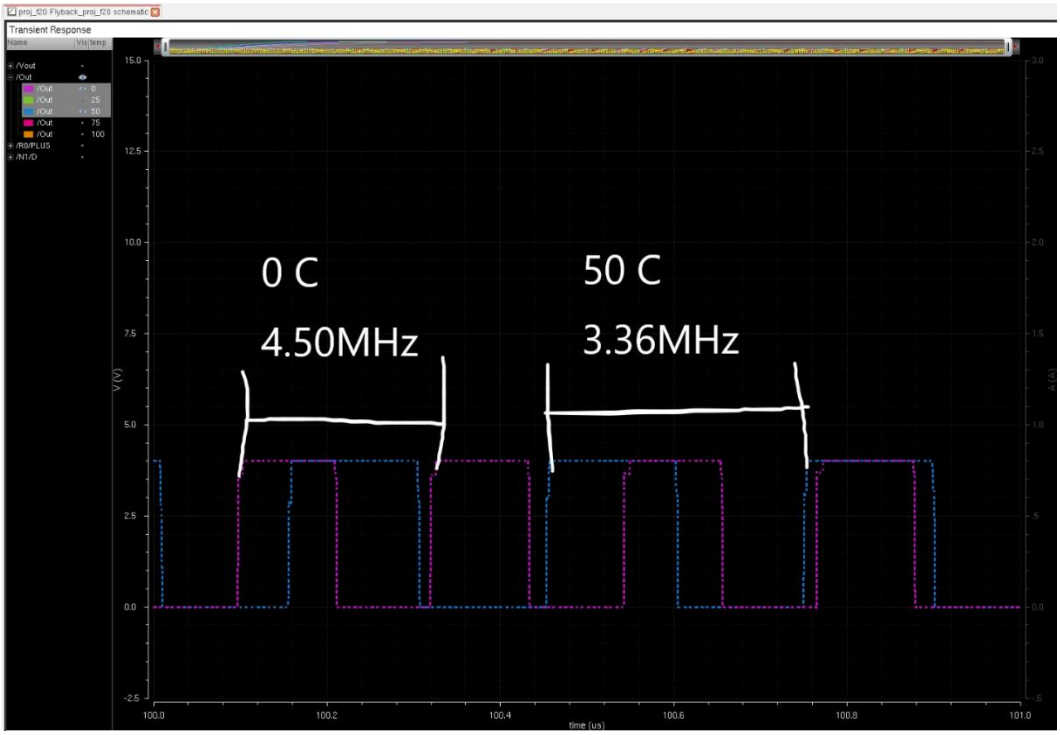
Temperature transient analysis (I_{input} @ 0 - 100℃) with the load of 5 Ω at 5V VDD

Temperature dependence measurement with the load resistance of 5Ω at 4V VDD							
Temperature	Minimum Voltage	Maximum Voltage	Ripple Voltage	Frequency	Input Power	Output Power	Efficiency
0℃	12.81V	13.23V	210mV	4.50MHz	36.96 W	33.55 W	90.77%
27℃	12.83V	13.24V	205mV	3.85MHz	37.25 W	33.64 W	90.31%
50℃	12.84V	13.19V	175mV	3.36MHz	38.44 W	33.68 W	87.62%
75℃	12.85V	13.15V	150mV	2.95MHz	40.43 W	33.68 W	83.30%
100℃	12.85V	13.12V	135mV	2.66MHz	43.04 W	33.67 W	78.23%

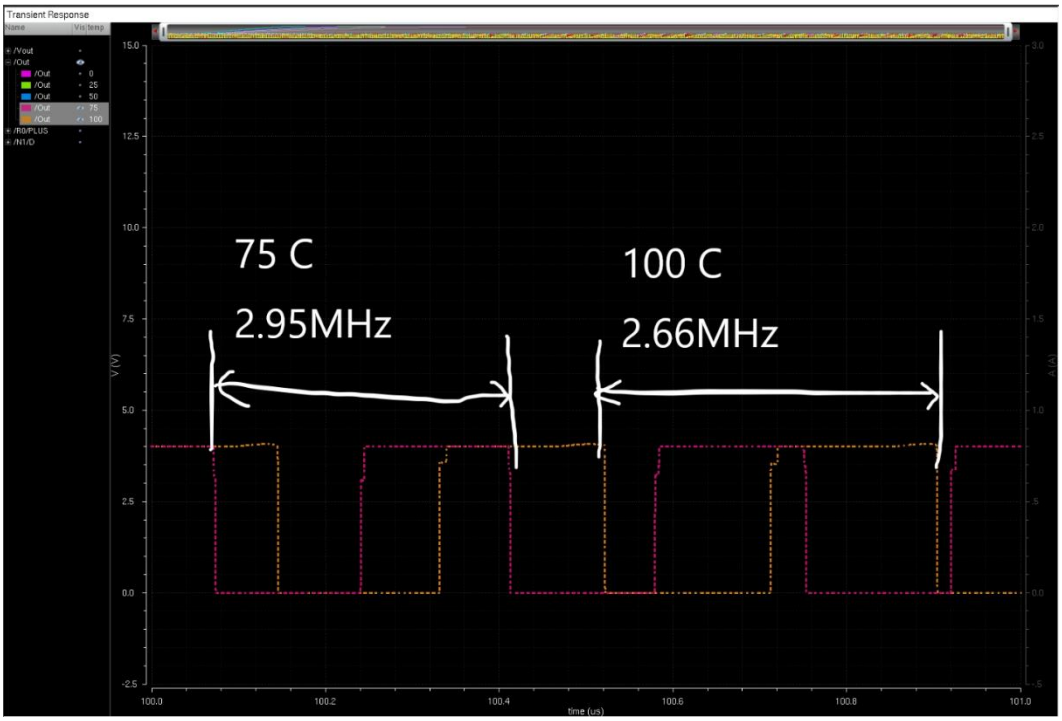
Additional temperature analysis was performed for the 4V VDD input which it has been shown to be within the acceptable range of operation. This analysis, strangely, showed no phenomenon that was observable from the 5V 0℃ in efficiency. This might point out that either the calculation of the efficiency from the 5V 0℃ was not correct.



Temperature transient analysis (Vout @ 0 – 100℃) with the load of 5 Ω at 4V VDD



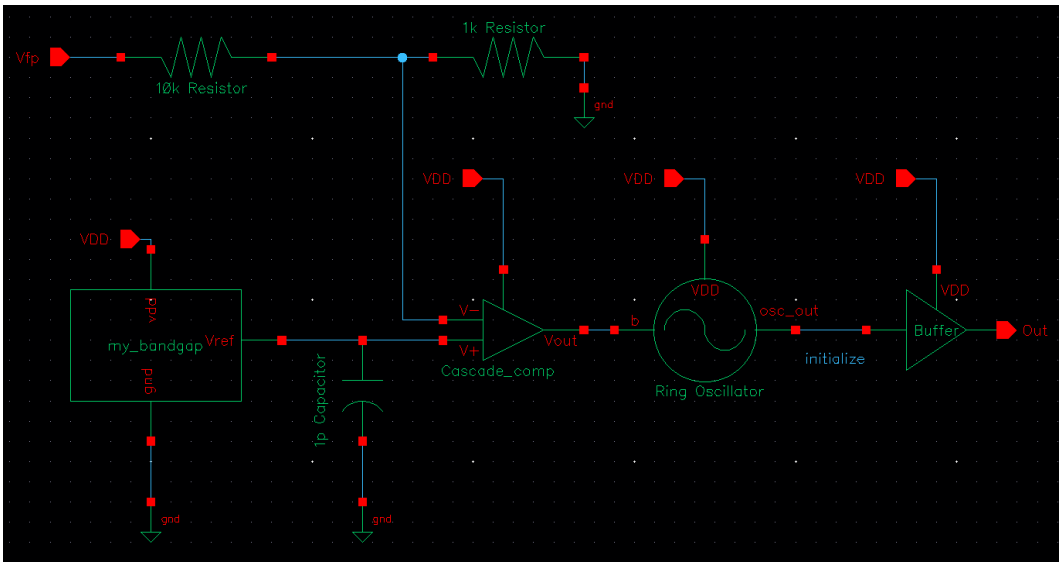
Temperature transient analysis (Out @ 0 vs 50℃) with the load of 5 Ω at 4V VDD



Temperature analysis (Out @ 75 vs 100°C) with the load of 5 Ω at 4V VDD

You can see that even though the VDD is decreased, the same variable relationship that was evident in 5V VDD can also be seen in 4V VDD.

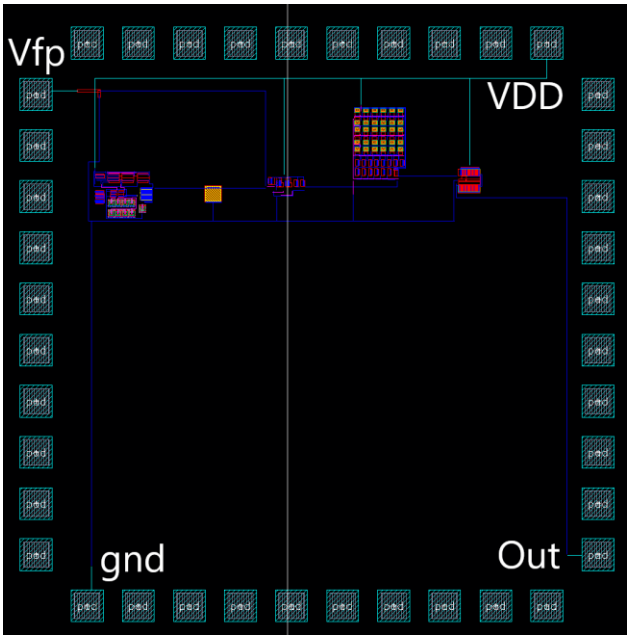
5. Chip schematic, layout, and results



Chip Schematic

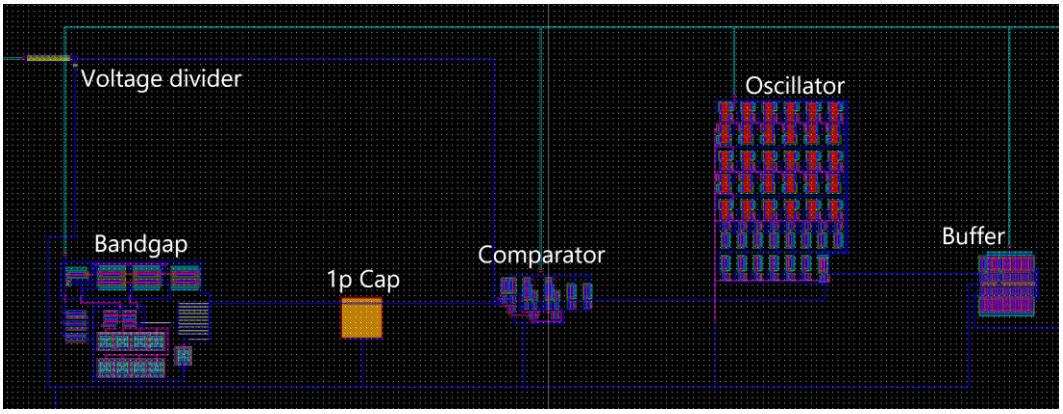
The schematic shown above, and all the components are designed and laid out with CMOS C5 process rules and sizes. Below is the datasheet for the C5 process.

CMOS C5 process specifications		
C'ox	R_n	R_p
2.5fF/μm^2	20kΩ	40kΩ



Chip Layout(with the pads)

The components are contained in a 10 by 10 chip size. However, the chip can be reduced in size since the components do not take much space and there's only 4 input/output pins needed (Vfp, Out, VDD, and gnd). Small components such as pads, hi-res resistors, and 1pF poly-poly capacitors are included in this section.

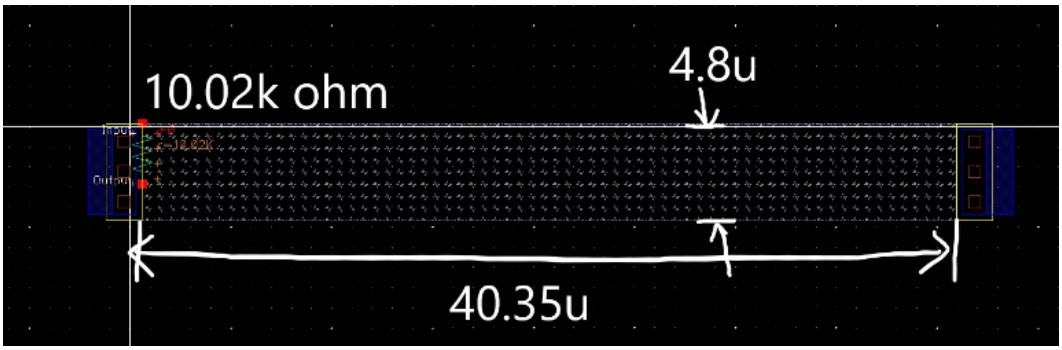


Chip Layout (zoomed in)

Upon close examination, the oscillator takes the greatest amount of space in this design. This is because the oscillator needs to output a rather fast 5MHz signal.

Chip LVS Result

5.1. 10k resistor schematic, layout, and result



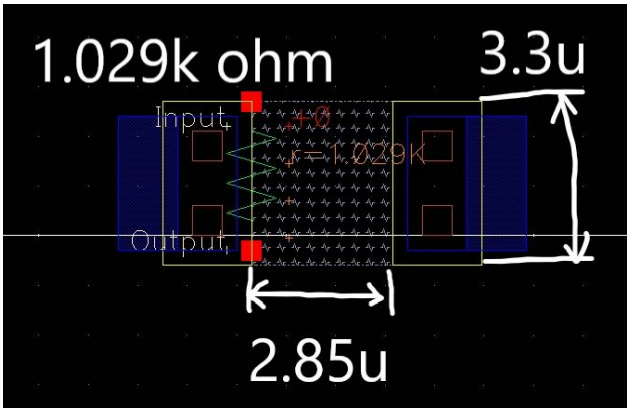
10k resistor layout

The poly layer was used to function as a hi-res resistor. The resistance of the hi-res resistor can be calculated with the equation below:

$$R = R_{square} \times \frac{L}{W} = 10k\ ohm\ =\ 1.19k \times \frac{40.35}{4.8}$$

The m1_elec via is 1.8u long, which was not added to the calculation.

5.2. 1k resistor schematic, layout, and result



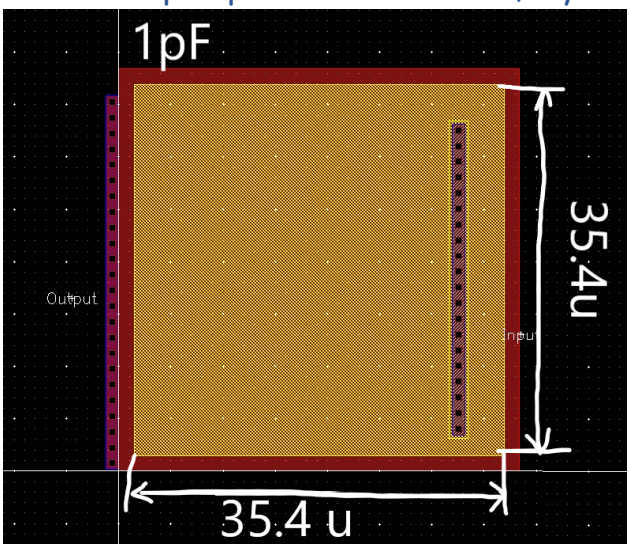
1k resistor layout

The same calculation can be done to achieve the 1kΩ as above.

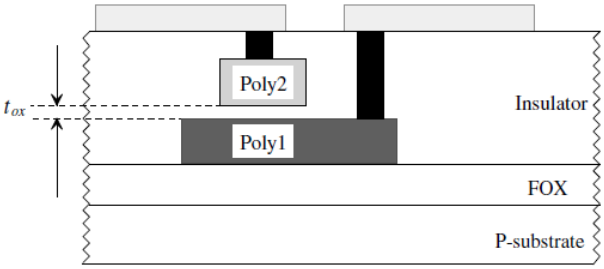
$$R = R_{square} \times \frac{L}{W} = 1k\ ohm\ =\ 1.19k \times \frac{2.85}{3.3}$$

Another way to design this part is to have 11 thinner resisters in a serpentine pattern and to have the 10th corner as the output. This has its own drawback of being more fragile due to the thinner body and less vias to be able to handle a large voltage or having more capacitance.

5.3. 1p capacitor schematic, layout and result



1p capacitor layout



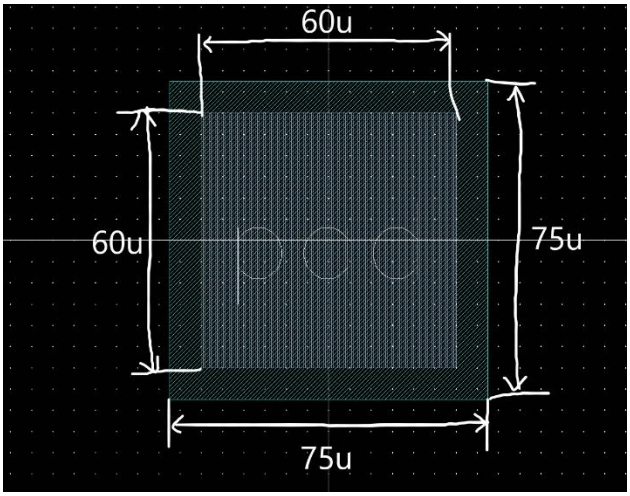
cross-sectional view

The poly-poly capacitor was used for the chip. To calculate the capacitance, the equation below was used.

$$C_{ox} = C'_{ox} \times A = 1pF = 2.5fF/\mu m^2 \times 20\mu m \times 20\mu m$$

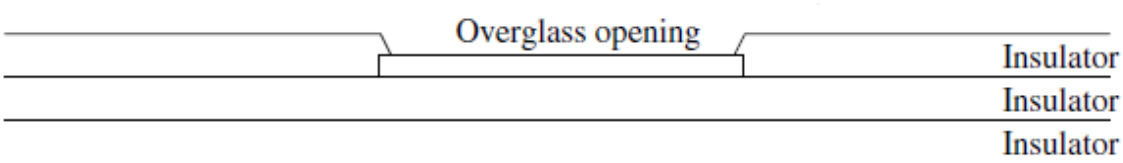
However, unlike the theoretical value of 20μm length and width, fine tuning has to be done according to the extracted result, making the length and width 35.4μm. This might has to do with the t_{ox} difference.

5.4. Pad schematic and layout

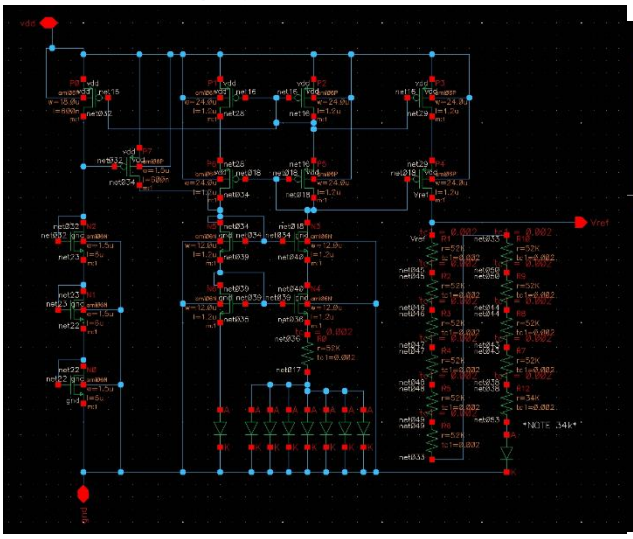


Pad layout

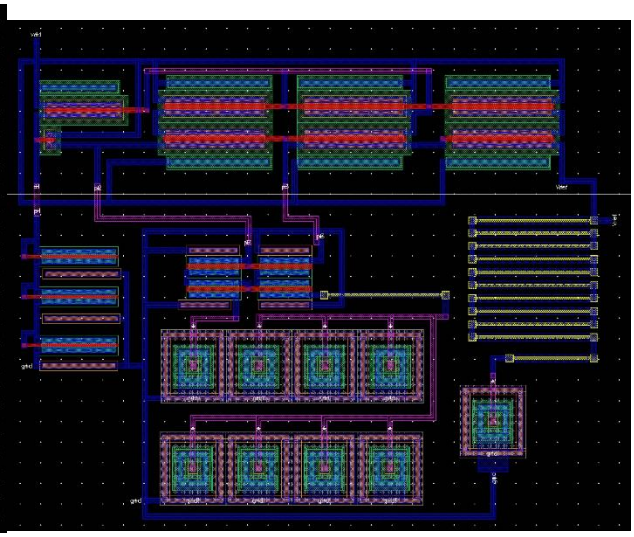
The pad has a 7.5μm spacing between the metal layer and the over glass layer. The standard (the CMOS book) spacing is 6μm. The below is the cross-sectional view of the pad.



6. Bandgap schematic, layout, and results

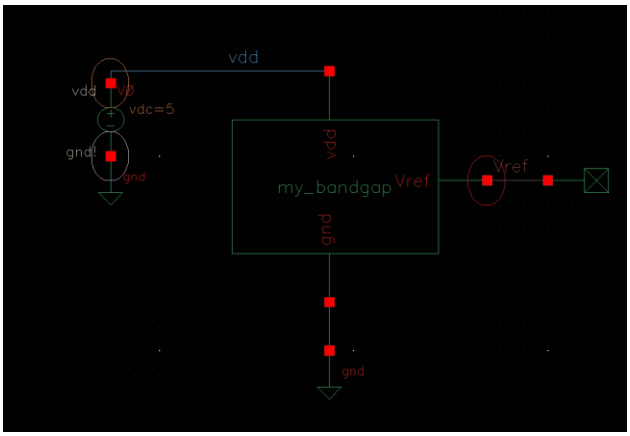


Bandgap schematic



bandgap layout

The bandgap functionality was outside the scope of the class. However, laying out the bandgap was. It has passed the LVS. Two trials of VDD and temperature testing was performed. The results are as shown below.

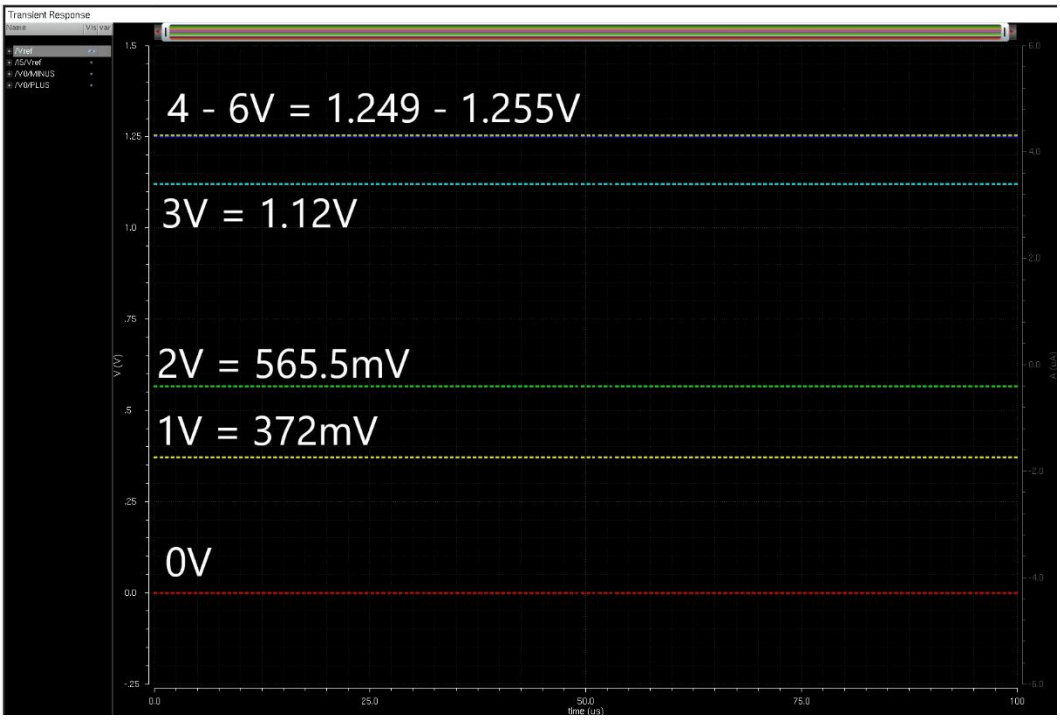


Bandgap testing schematic

6.1. VDD parametric analysis on bandgap

VDD vs Vref vs Power of bandgap		
VDD	Vref	Power
0V	0V	~0W
1V	372.0mV	6.508pW
2V	565.5mV	8.473nW
3V	1.12V	6.484µW
4V	1.249V	11.66µW
5V	1.252V	17.07µW
6V	1.255V	29.39µW

As you can see from the data above, the functional range of the bandgap is from 4V to 6V. However, the optimal operating voltage is close to 4V because it outputs a voltage closer to 1.25V. It can also be seen that the higher the power the more power it consumes. On top of that, it can be expected to have a higher hysteresis at 5V VDD because it is roughly 50mV higher than desired. This might contribute to the higher hysteresis of the chip at 5V operation.

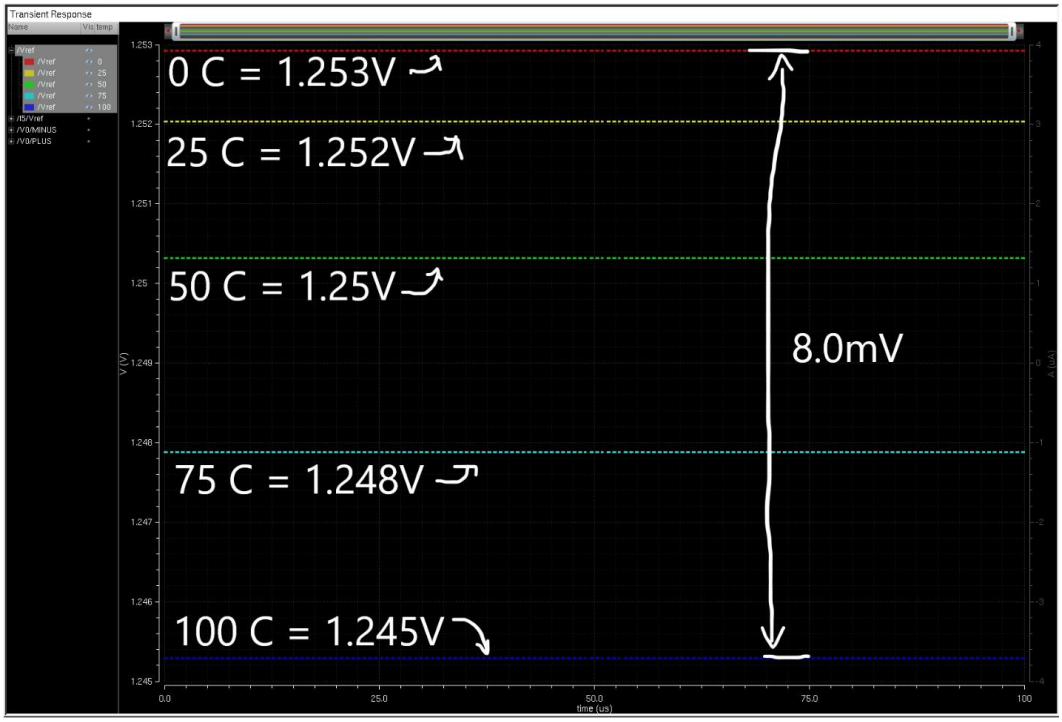


VDD transient analysis (Vref @ 0 – 6V VDD) at 27℃

6.2. Temperature parametric analysis on bandgap

Temperature vs Vref on bandgap		
Temperature	Vref	Power
0℃	1.253V	16.72μW
25℃	1.252V	17.05μW
50℃	1.25V	17.36μW
75℃	1.248V	17.63μW
100℃	1.245V	17.91μW

The temperature analysis was done under 5V VDD source. The data shows that temperature has a negative relationship with the output voltage Vref. However, it increases the power use even though the output voltage is lowered.



Temperature transient analysis(Vref @ 0 – 100℃) with 5V VDD

Even thought there is a correlation between the temperature and the output voltage, it can be concluded that it does not matter since the difference is going to be less than 8mV. Therefore, temperature is negligible in terms of the bandgap functionality.

7. Comparator schematic, layout, and results

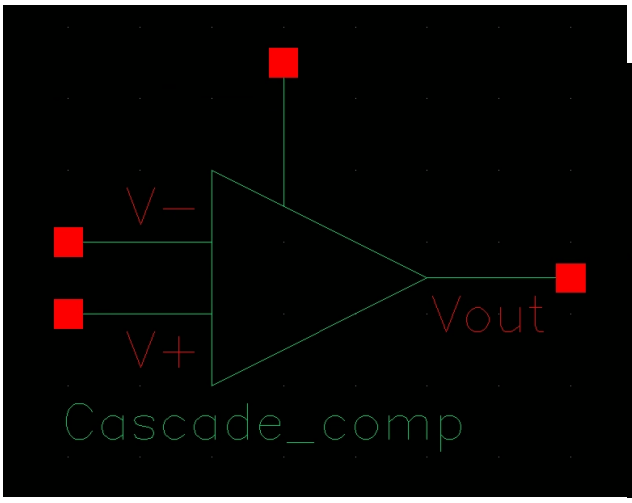
Comparator is cascaded to give a better result than a single comparator. Then the output is taken from the positive side and its edges have been sharpened by the two fast inverters. Below is the ideal comparator truth table.

Ideal comparator truth table	
V+ > V-	V+ < V-
5V	0V

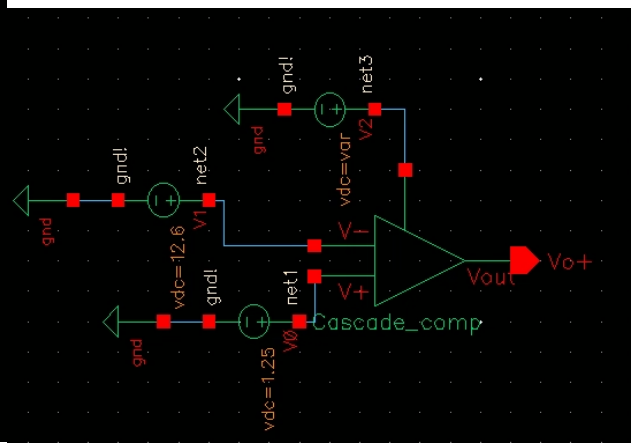
Comparator is the single most important component in the chip that determines the ripple voltage. As you can see from the schematic and the layout, mismatching size of the PMOSes were used to fine tune the final voltage outcome. This is because the switching point formula is dependent on the ratio of the β_n and β_p of the CMOS. The formula used is below.

$$V_{SP} = \frac{\sqrt{\frac{\beta n}{\beta p}} \times V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta n}{\beta p}}}$$

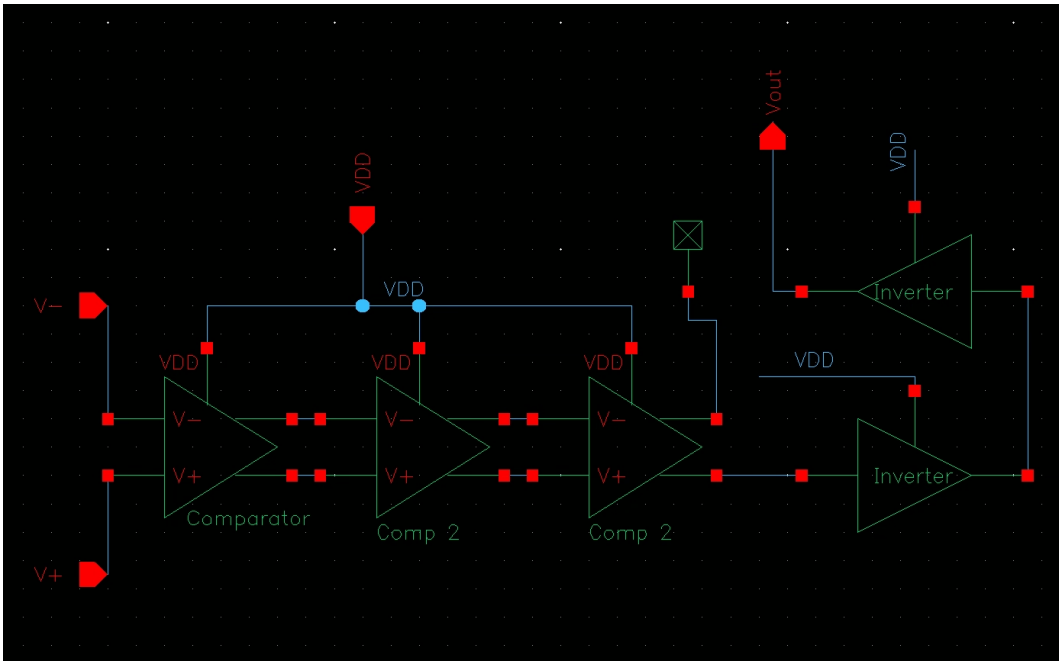
Switching point is where the input voltage is equal as the output voltage. Because lowering the β_p increases the switching point, the comparator's switching point is lowered in that manner. Another way to lower the switching point is to use a long channel NMOS. However, this would consume more power.



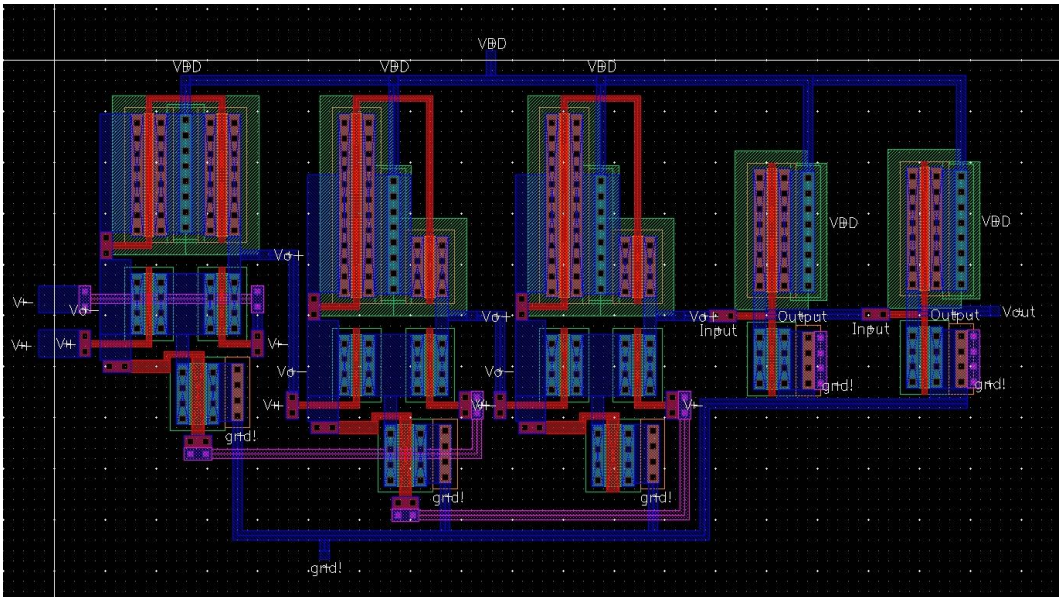
Cascade comparator symbol



Cascade comparator simulation setup



Cascade comparator schematic

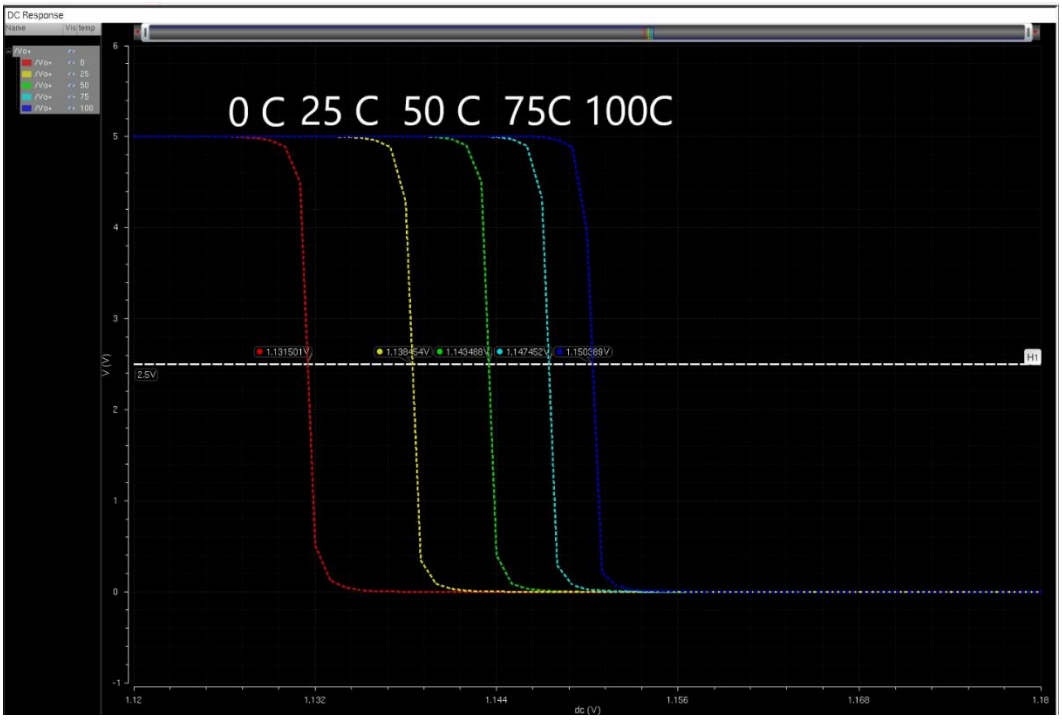


Cascade comparator layout

To observe the switching behavior, DC analysis was performed, and below are the results.

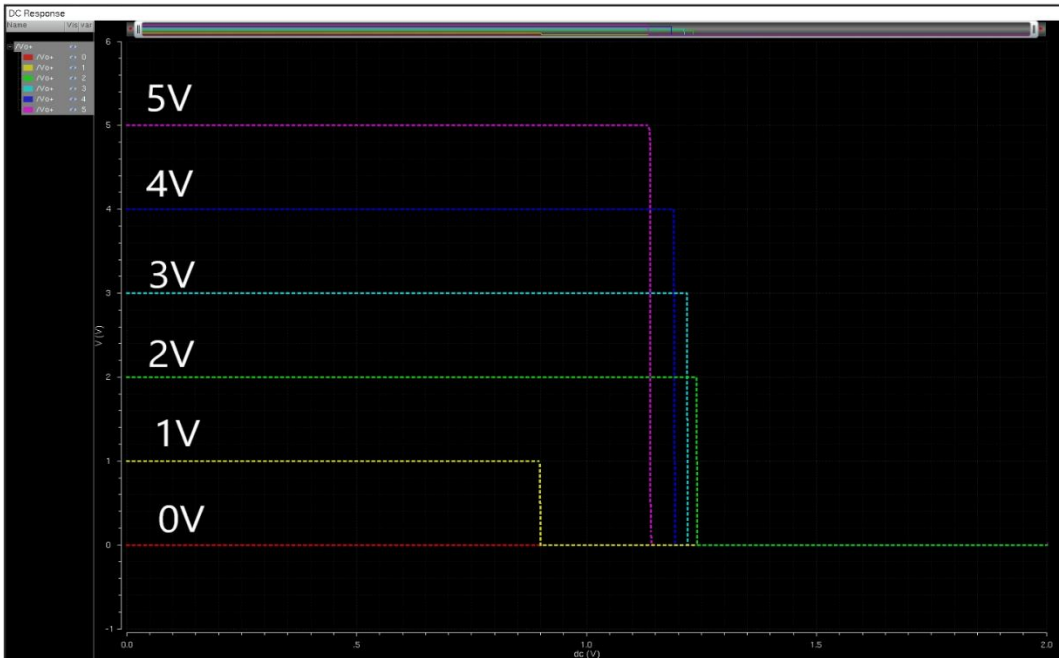
Switching point vs temperature		
Temperature	Switching point	Power
0℃	1.132V	826.6μW
25℃	1.138V	903.6μW
50℃	1.143V	990.5μW
75℃	1.147V	1.09mW
100℃	1.150V	1.202mW

The data shows that the switching point goes up as the temperature goes up as well as the power. This explains the decrease in ripple because the temperature increase lowers the bandgap output and increases the switching point, making them close to switch the comparator output.



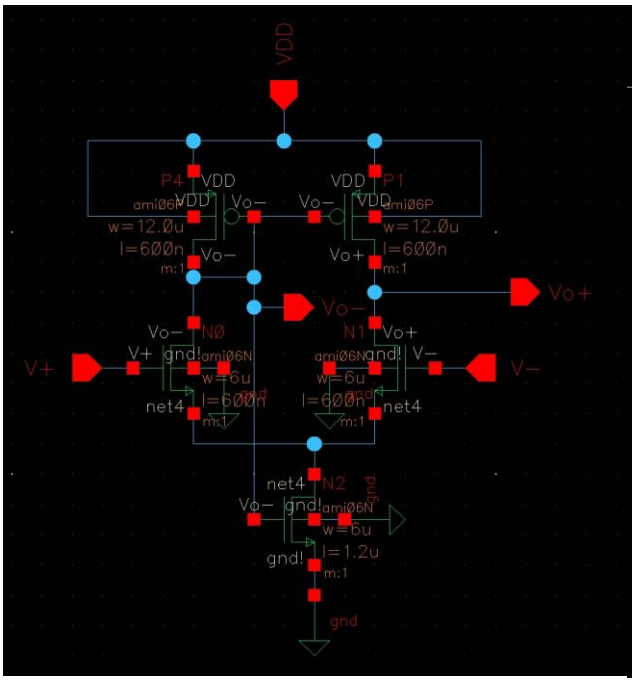
Temperature parametric DC analysis of the cascade comparator

Below is the VDD parametric analysis result. It seems that the switching point increases as the VDD decreases except for 1V. It is interesting to note that the output voltage is directly proportional to the input VDD voltage.

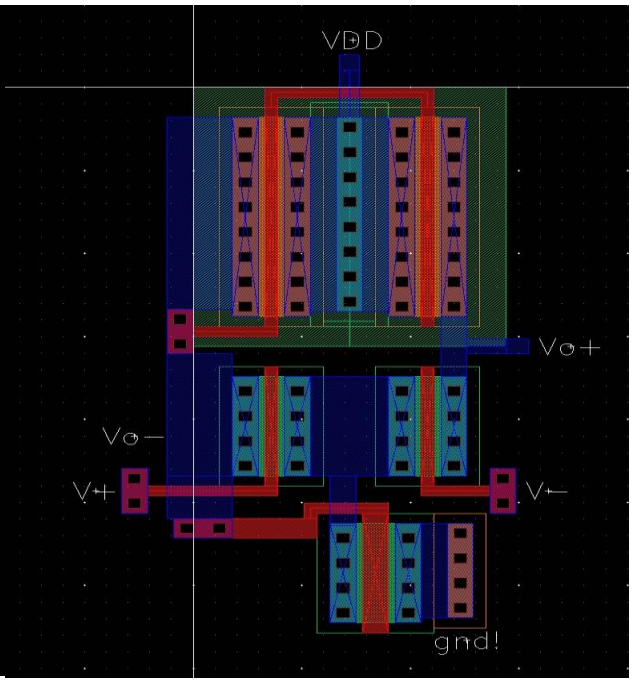


VDD parametric DC analysis of the cascade comparator output

7.1. Comparator 1 schematic, layout, and symbol



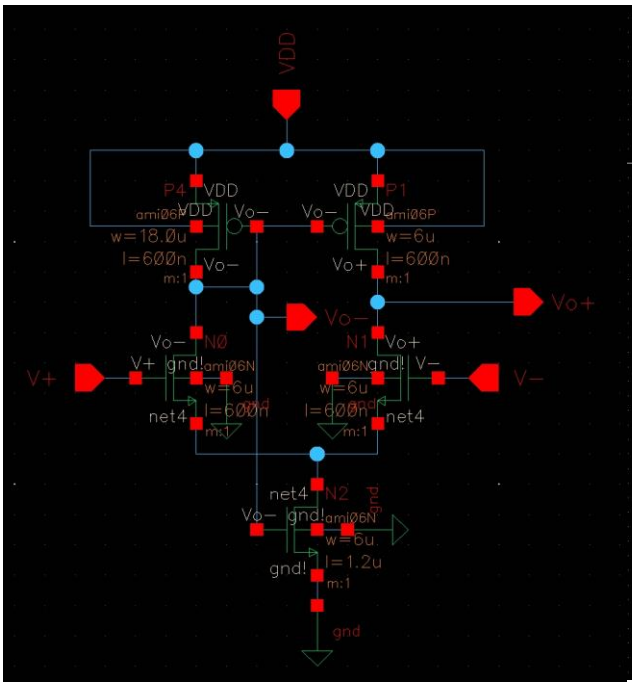
Comparator 1 schematic

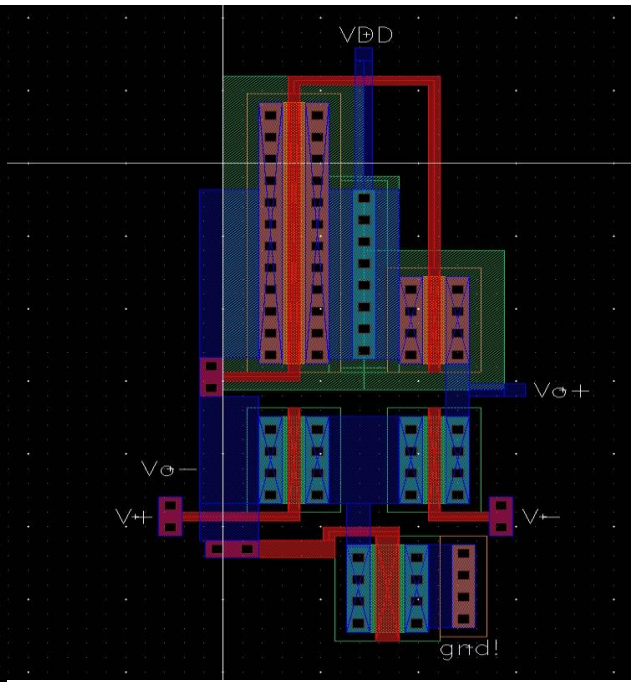


Comparator 1 layout

The first comparator used has the identical PMOS size. For the layout, a different approach has been tried and the body of the PMOS is shared in between the PMOSes. At least two vias are used for each connection to decrease the failure rate.

7.2. Comparator 2 schematic and layout



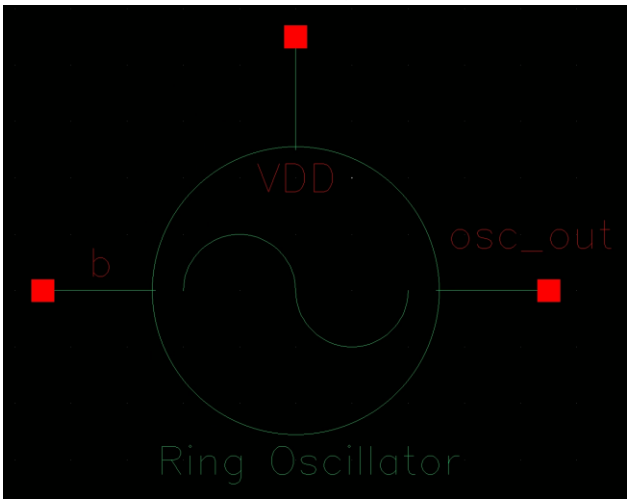


Comparator 2 schematic

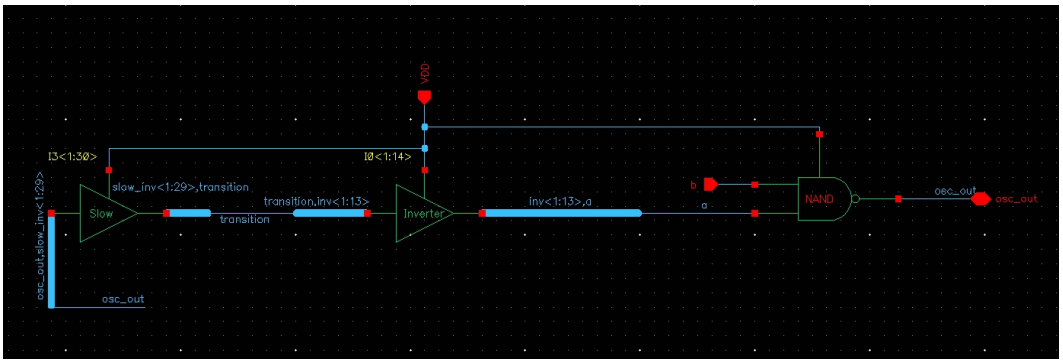
Comparator 2 layout

The second comparator has a smaller PMOS so that the switching point can be increased. Two of these comparators are used in cascade before the fast inverters. Fast inverter design will be under the ring oscillator section, which is the next section.

8. Ring oscillator schematic, layout, and results



Ring oscillator symbol



Ring oscillator schematic

The ring oscillator is consisting of 29 slow inverters and 14 fast inverters in series. The slow inverters are the major factor to set the oscillation frequency and period. Frequency and period are inversely related with the formula below:

$$Period(s) = \frac{1}{f} = \frac{1}{5MHz} = 200ns$$

The delay and the number of inverters needed can be calculated with the formula below:

$$C_{ox,slow} = \frac{2.5fF}{\mu m^2} \times 6\mu m \times 6\mu m = 90fF$$

$$C_{tot,slow} = \frac{5}{2}(90fF + 90fF) = 450fF$$

$$t_{PLH} = 0.7 \times 40k \times 450fF = 12.6n$$

$$t_{PHL} = 0.7 \times 20k \times 450fF = 6.4n$$

$$n = \frac{1}{f \times (12.6n + 6.4n)} = \frac{1}{5MHz \times 19ns} = 10.53 \approx 11\ slow\ inverters$$

However, it was more complicated than the simple calculation because there were two different types of inverters. For that reason, it was far more accurate to use trial and error to figure out the right inverter amount. That amount was 29 inverters. The design needs an odd number of inverters, therefore the number of fast inverters had to be even.

The fast inverters are the major factor to set the rise/fall time. Rise/fall time is calculated by the formula below:

$$C_{oxp,fast} = \frac{2.5fF}{\mu m^2} \times 12\mu m \times 0.6\mu m = 18fF$$

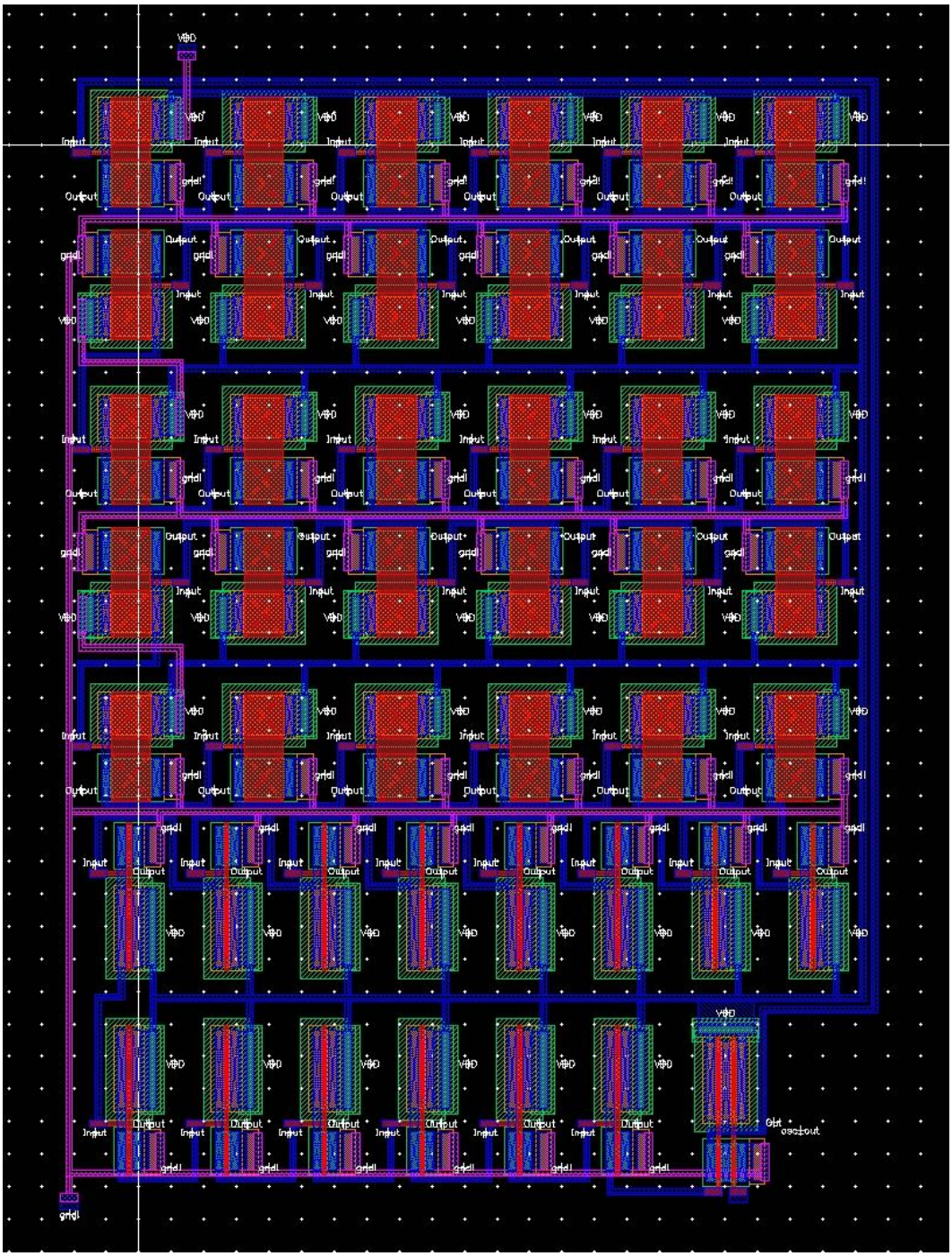
$$C_{oxn,fast} = \frac{2.5fF}{\mu m^2} \times 6\mu m \times 0.6\mu m = 9fF$$

$$C_{tot,slow} = \frac{5}{2}(18fF + 9fF) = 67.5fF$$

$$t_{PLH} = 0.7 \times 40k \times 67.5fF = 1.89n$$

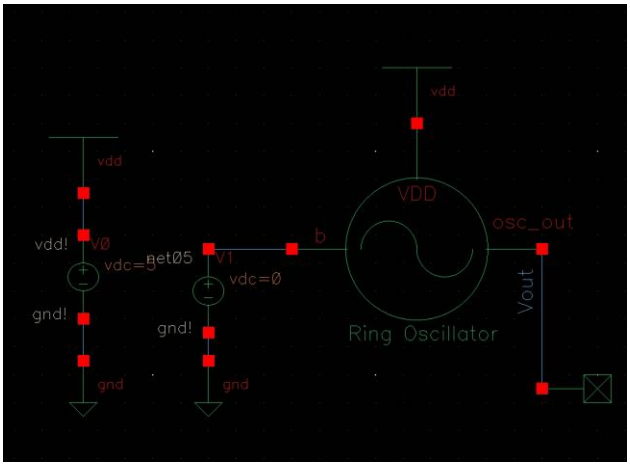
$$t_{PHL} = 0.7 \times 20k \times 67.5fF = 0.945n$$

The average rise and fall time were about 1.4ns, which is an acceptable range of operation. Using the same equation used for the slow inverters, 14 fast inverters gives the frequency of 25MHz.



Ring oscillator layout

The ring oscillator layout was going to be the largest component in the chip. Therefore, a special attention has been given to minimize the layout size.

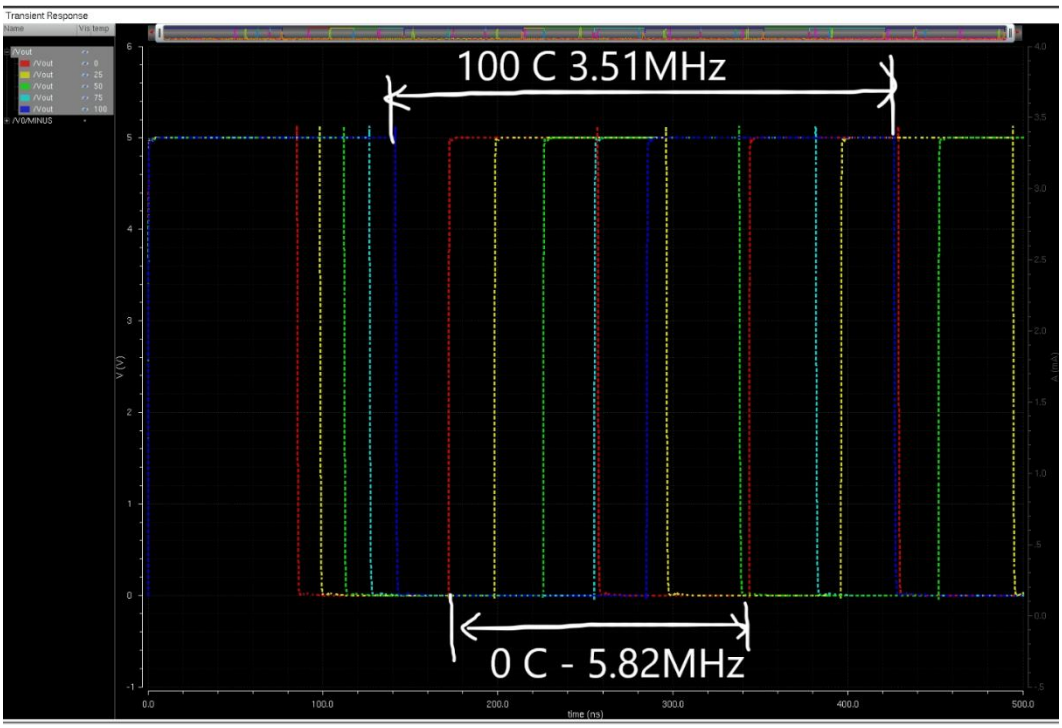


Ring oscillator test schematic

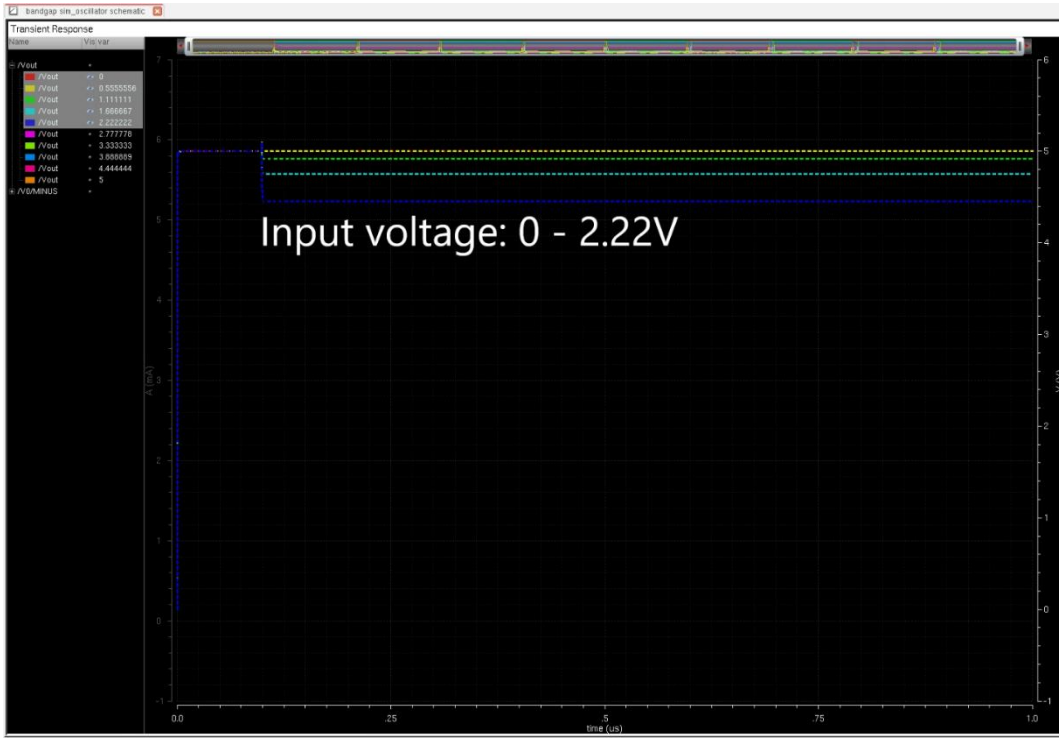
Temperature vs frequency with 5V input		
Temperature	Frequency	Power
0℃	5.82MHz	1.1mW
25℃	5.05MHz	966.3μW
50℃	4.43MHz	835.6μW
75℃	3.92MHz	739.2μW
100℃	3.51MHz	672.3μW

The results show that as the temperature goes up the frequency goes down. Strangely, the power also went down. This might be from the fact that the slower the oscillation the less power it is to be required. The temperature's effect on the frequency is visualized with the graph below.

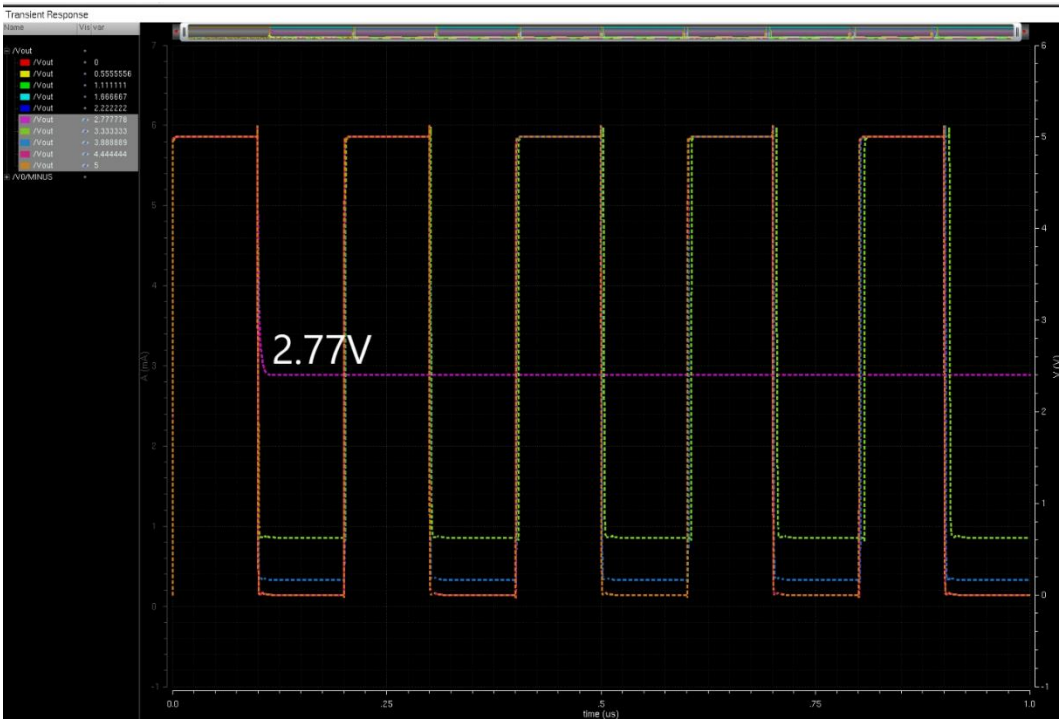
Another analysis was done with the input voltages. The result shows that the VDD below 2.77V were within the undesirable realm because it either output a constant 5V or does not fully oscillate down to 0V. The VDD of 3.33V and up were functional with the desired frequency. However, voltages lower than 5V does not fully reach the 0V oscillation despite they reach the 5V. Because of this fact, it should not affect the function of the chip at 4V.



Temperature parametric analysis of the ring oscillator for 5V input

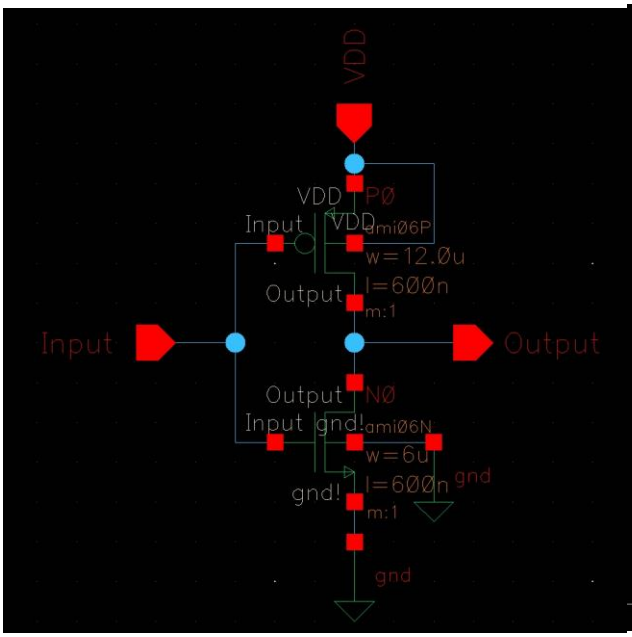


Input voltage parametric analysis(0-2.22V) of the ring oscillator at 27°C

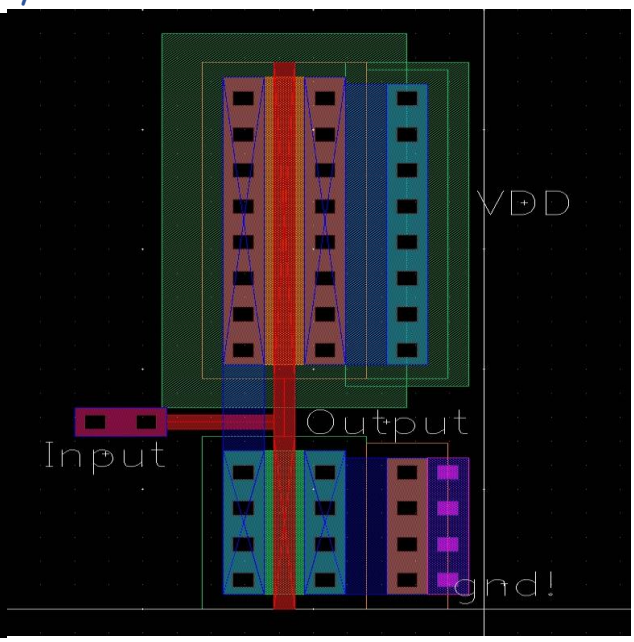


Input voltage parametric analysis (2.77-5V) of the ring oscillator at 27℃

8.1. Fast inverter schematic and layout

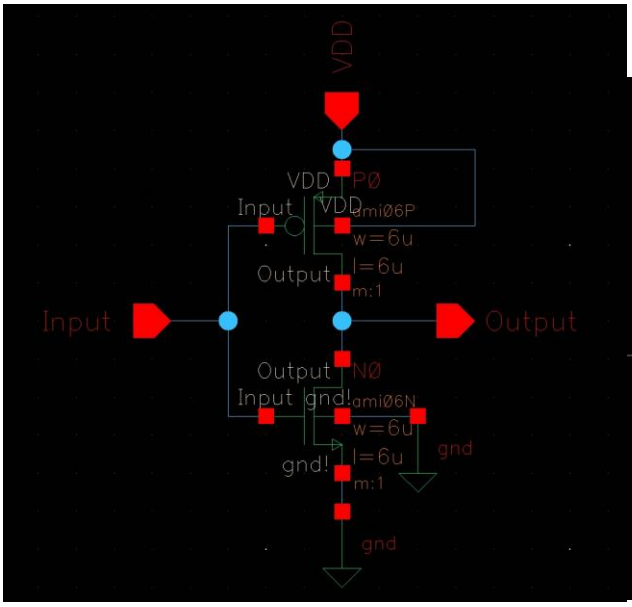


Fast inverter schematic

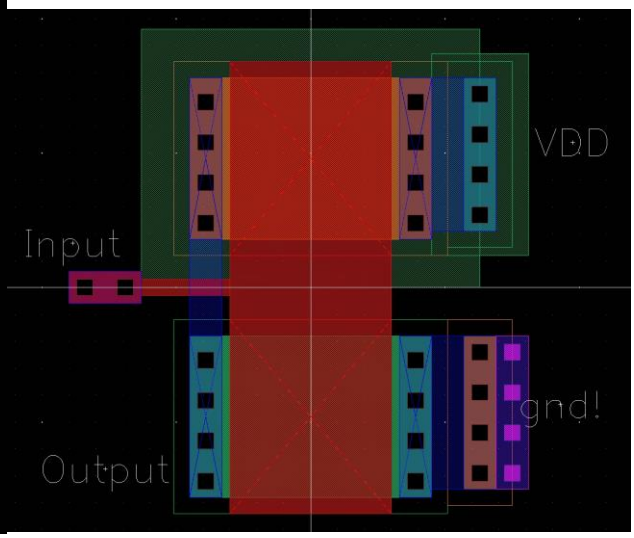


Fast inverter layout

8.2. Slow inverter schematic, layout, and result



Slow inverter schematic



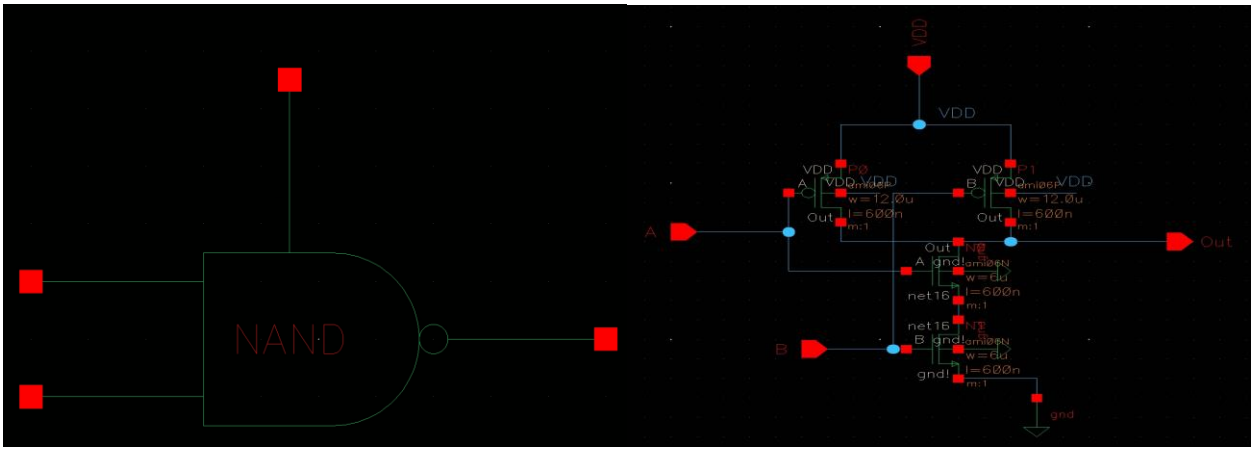
Slow inverter layout

8.3. NAND2 schematic, layout, and result

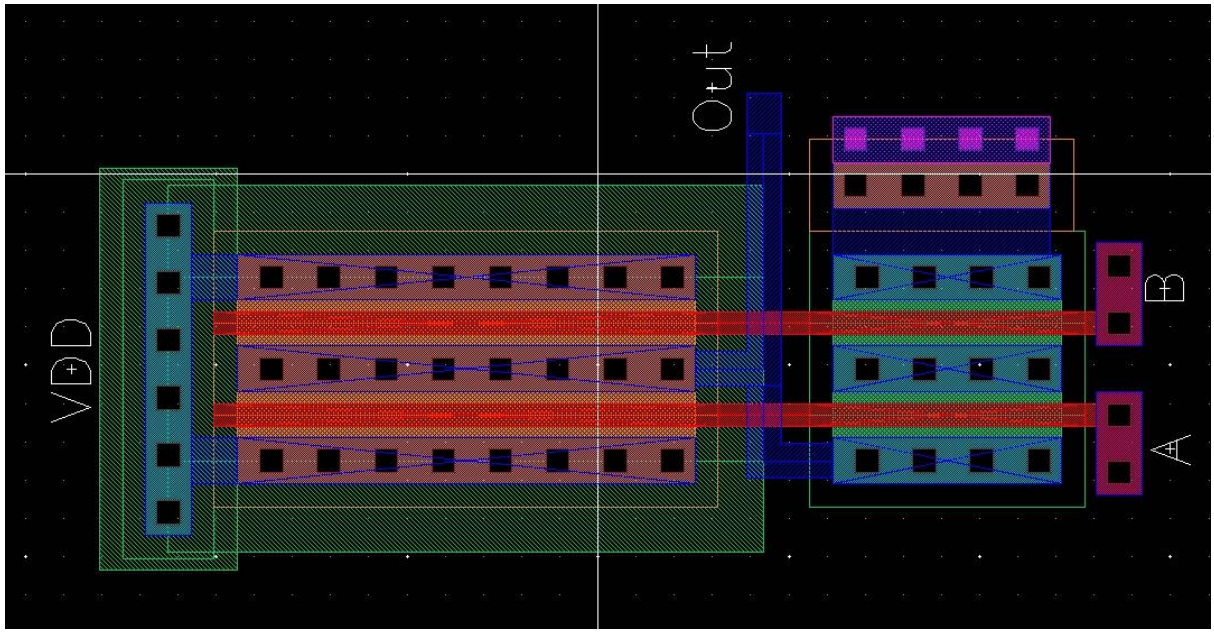
The operation of NAND2 gate is explained in the truth table below:

The operation of the ideal NAND gate		
A	B	Out
0	0	5V
0	1	5V
1	0	5V
1	1	0V

The NAND2 gate has 2 inputs (hence the 2 in the name): one is connected to the oscillator and the other is the function of the NAND2 gate is to output the oscillation only when the input from the oscillator is high (low on charge) and output the constant 5V when the input is low (sufficiently charged). This 5V output will be inverted and will be buffed at the buffer stage to be 0V (no charge on the device).



NAND2 symbol NAND2 schematic

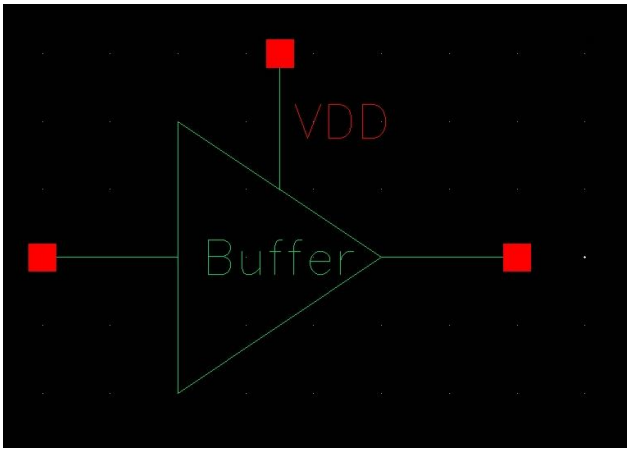


NAND2 layout

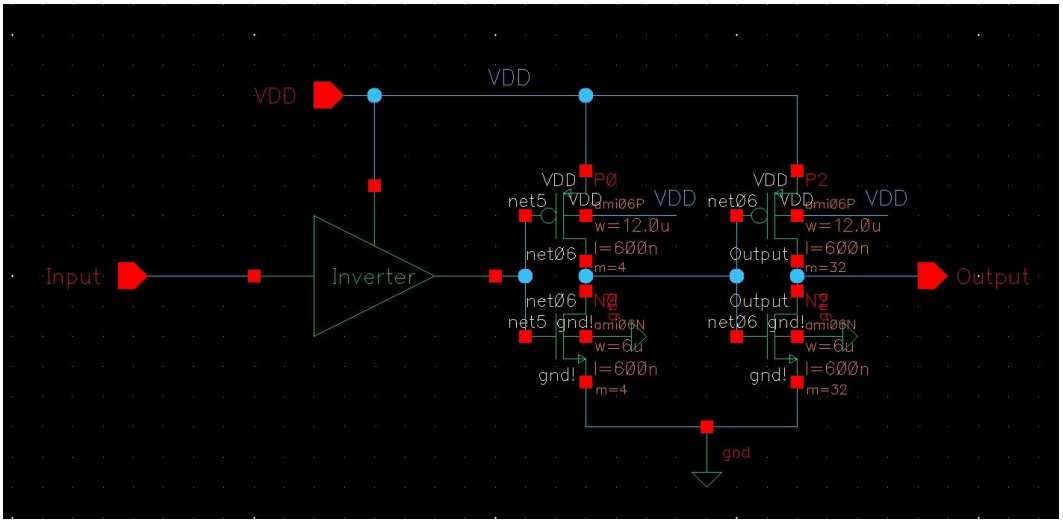
The future improvement can be made to fine-tune the ring oscillator according to the top function, as the individual analysis showed oscillation close to 5MHz, but the top function had a higher oscillation. This can be solved by adjusting the ring oscillator at the top function by descending to the component.

9. Buffer schematic, layout, and results

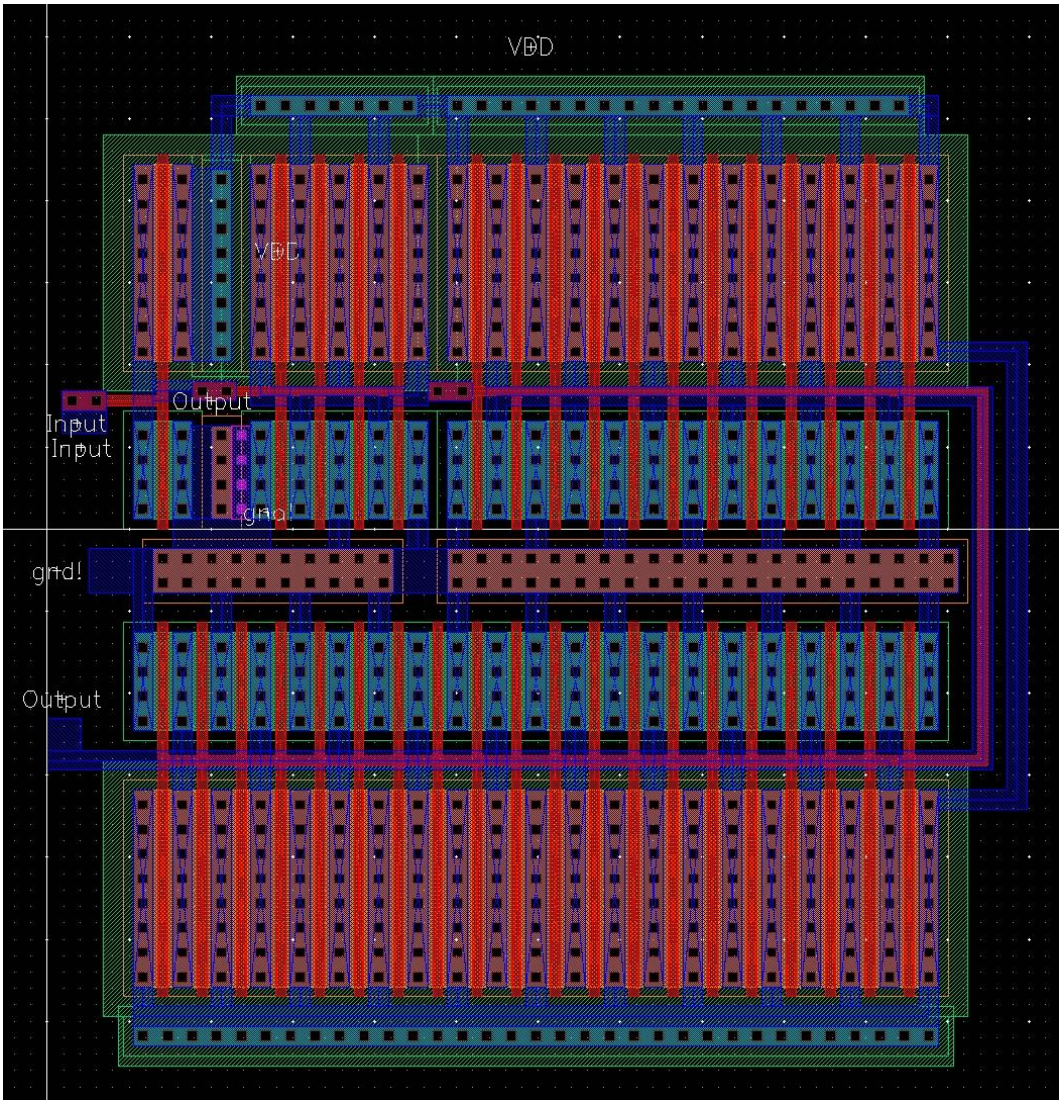
The role of the buffer is the simplest of all: to buff the current. This buffer has an increment constant of 4 for the second buffer and the constant of 8 for the third buffer to drive a larger current with a smaller number of inverters. Also, the constant could have been 8 to begin with. However, the compensation for that would be larger power consumption.



Buffer symbol

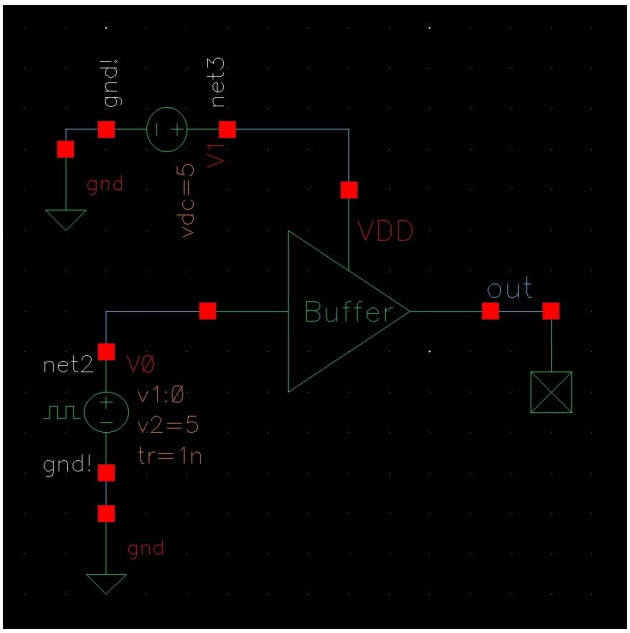


Buffer schematic



Buffer layout

A considerable effort was put into designing the buffer layout to be not as long for space saving. The layout technique utilized here was that the longest inverter is split in half and put under while it is still being connected as one.

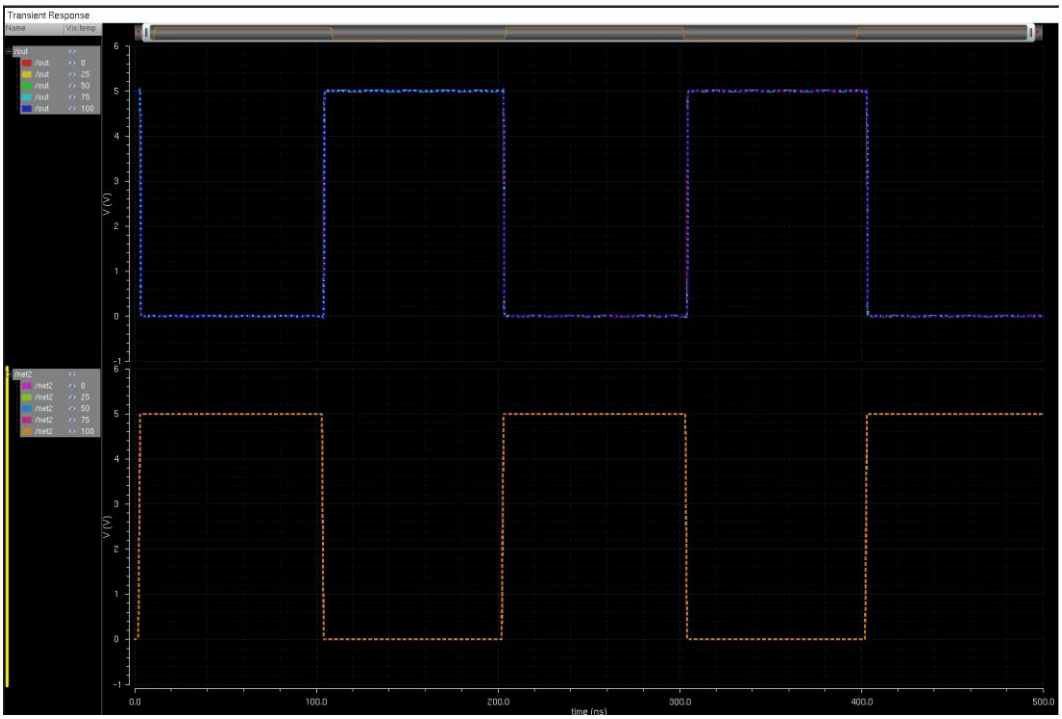


Buffer test schematic

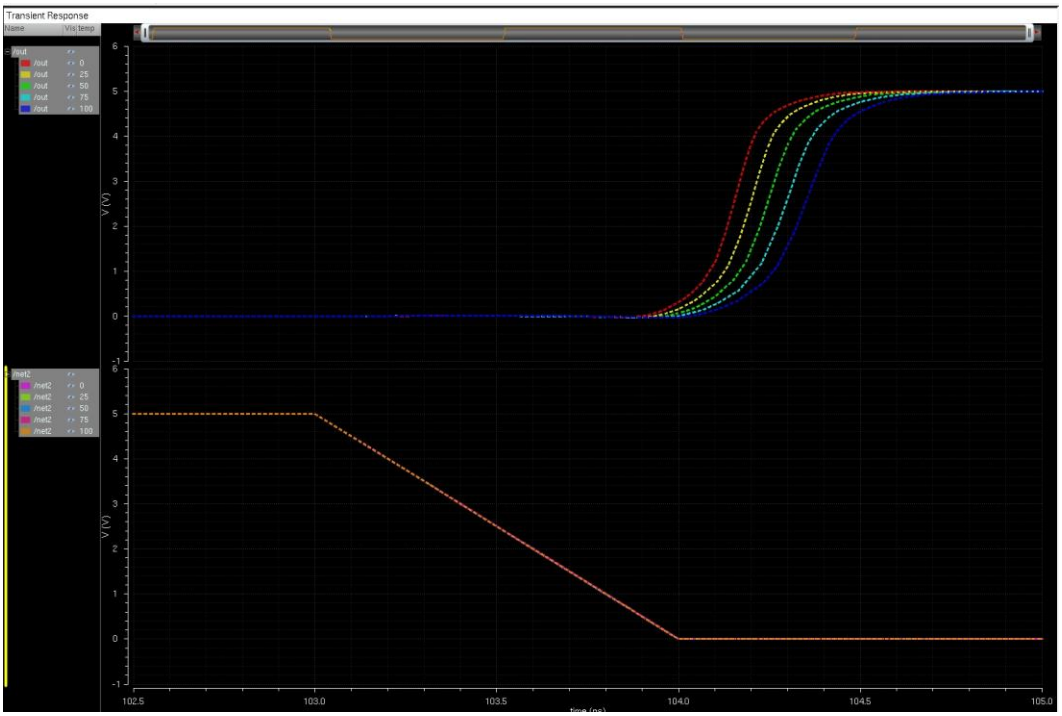
Temperature	Power
0℃	605.5μW
25℃	595.8μW
50℃	587.4μW
75℃	578.5μW
100℃	571.3μW

For the temperature analysis, the only thing that varied was the power. As the temperature goes up, the power went up. This might be explained by the fact that the threshold voltage decreases as the temperature increases. This means that the device performance increases as the temperature goes up. This also means that the device in the lower temperature can effectively buff the current better than in the higher temperature, consuming more power.

As the graph below shows, the buffer is consisting of stronger inverters that the temperature change does not show much variation in the output. Another graph displays the effect of temperature to the switching time, but as the graph shows, it is quite negligible. It is important to note, however, that there is a positive correlation between the temperature and the switching time/delay.



Temperature parametric analysis of the buffer with 5V VDD and input.



Temperature parametric analysis of the buffer with 5V VDD and input(closeup)

10. Conclusion & future work

The chip design had a considerably large ripple, but the operation was as desired. It did not overcharge much, and it did not constantly charge as well. Also, the chip did not consume much power. It also was not as much temperature dependent.

There were few things that can obviously be improved. First, the bandgap can be modified to output a reference voltage close to 1.25V. However, the bandgap used in the project was good enough for most of the case, and this improvement is not urgent.

What is urgent is in the comparator and oscillator design. Even though the comparator was tuned after the chip was assembled so it could take into consideration of all the combined components, the oscillator had little change after it was tested individually and assembled with the other components. Because of that, the oscillation at the ideal condition was a bit faster (+0.7MHz) than what was desired. Another improvement to the comparator that could be made is to utilize more inverters to sharpen up the rises and falls of the component to help achieve a better ripple voltage. Another way to reduce the ripple voltage is to cascade more comparator. The obvious drawback is the decrease in power efficiency. But considering the device has achieved a near 98% efficiency in the ideal state, a little bit of compensation won't drive the chip out of competition.

Another improvement that can be made is in the oscillator. As mentioned above, the small modification to the oscillator after the assembly would make the output closer to the desired frequency. This alteration could be reducing the number of slow oscillators since they are the ones that affect the frequency the most.

Buffer design was not problematic however its size can be modified according to the new and improved specifications required.