Active and Passive Microwave Engineering

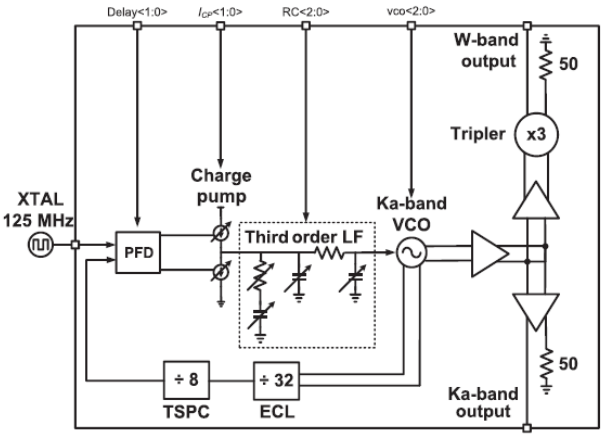
Final Project

ECG633

Cho Minsung

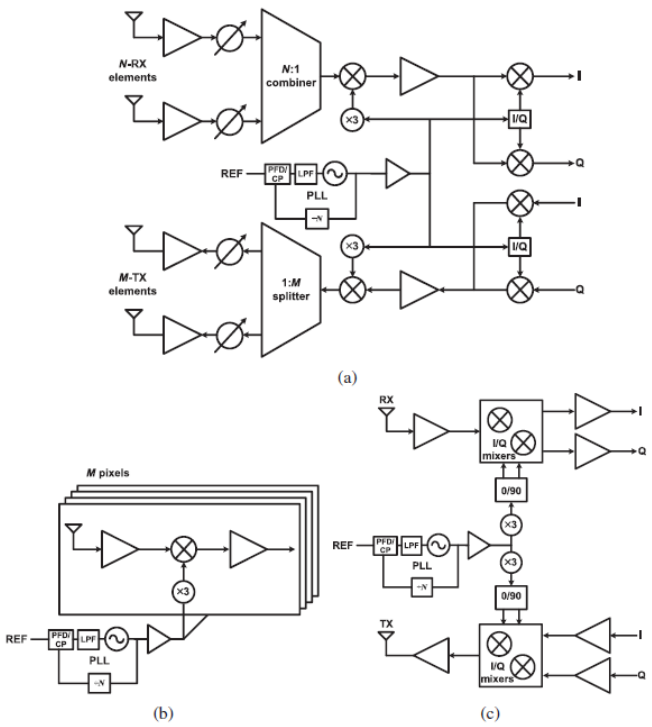
Millimeter-wave Frequency Synthesis Based on Frequency Multiplications

Introduction and Motivation

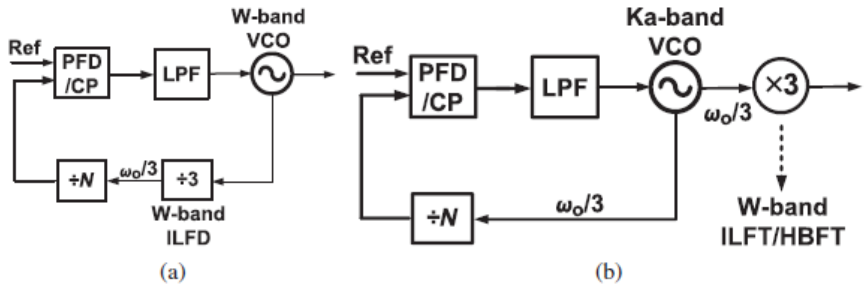


A critical component in W-band imaging system, automotive radars, point-to-point data communication, and 100 Gbps Ethernet is the frequency synthesizer. The W-band of the microwave part of the electromagnetic spectrum ranges from 75 to 110 GHz. As the operation frequency increases, the implementation of low phase-noise oscillators with adequate tuning range and output power will become increasingly difficult. One solution is to use a frequency multiplier, proceeded by a lower-frequency phase-locked loop(PLL). A PLL is a control system that generates an output signal whose phase is related to the phase of an input signal.

The Ka-band PLL is comprised of a differential Colpitts VCO, a frequency divider chain with the division ratio of 256, a phase frequency detector(PFD), a clock pulse(CP), and a third-order loop filter. Programmable PFD delay (Delay<1:0>), CP current (Ic<1:0>), and loop BW (RC<2:0>) compensate for model inaccuracy and PVT variation. The W-band signal is synthesized by cascading a frequency tripler after a Ka-band (30.3 through 33.8 GHz) PLL. Chip A incorporates the injection locked frequency tripler (ILFT), whereas Chip B uses the harmonic-based frequency tripler (HBFT) after the PLL. XTAL is a crystal. PHD is a phase frequency detector. TSPC is a true single-phase clock. ECL is an emitter-coupled logic. VCO is a voltage controlled oscillator.



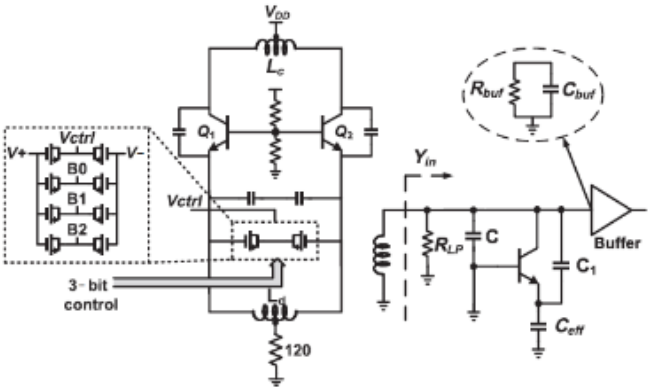
Right side illustrates three possible LO generation and distribution schemes that can be implemented using the PLL system depicted above. (a) is a dual-conversion zero-intermediate-frequency(IF) superheterodyne 120GHz phased-array transceiver. (b) shows M-pixels 94GHz direct-conversion passive imaging. A direct-conversion 84GHz transceiver(TRX) for active imaging/communication is depicted in (3).



There are three different approaches for W-band frequency synthesis: (1) using a W-band fundamental PLL, as shown

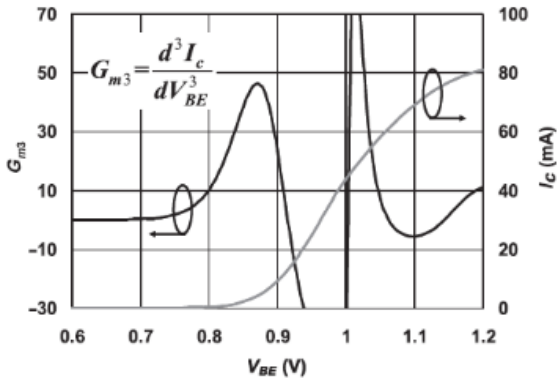
below as (a), (2) using a Ka-band PLL cascaded with an ILFT, and (3) using a Ka-band PLL cascaded with an HBFT, as shown above as (b). The fundamental PLL means the PLL's output frequency being equal to the fundamental frequency of the VCO. By comparing (a) and (b), we notice that two building blocks are different: the W-band PLL employs a W-band VCO and an injection-locked divider-by-3 (ILFD), whereas the other system employs a Ka-band VCO and an ILFT. An ILFD consumes the same amount of power as the Ka-band VOC in (b).

Design of a Silicon-Based Ka-Band PLL



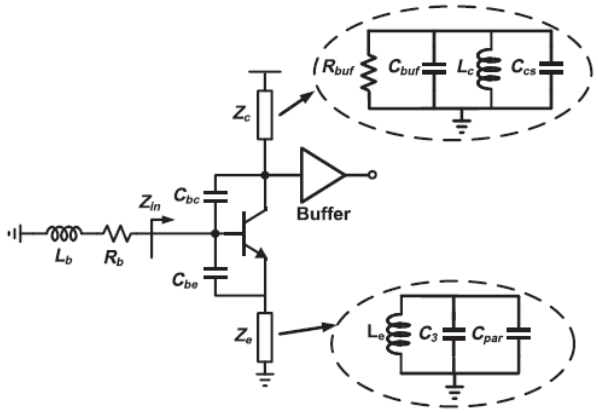
The figure shows the VC schematic where a differential Colpitts topology with emitter degeneration is chosen for better phase noise performance. VCO employs a 3-bit digital band selection in addition to an analog varactor control. Also, shown in the figure is a simplified half-circuit equivalent model of the VCO.

Design of a W-Band ILFT

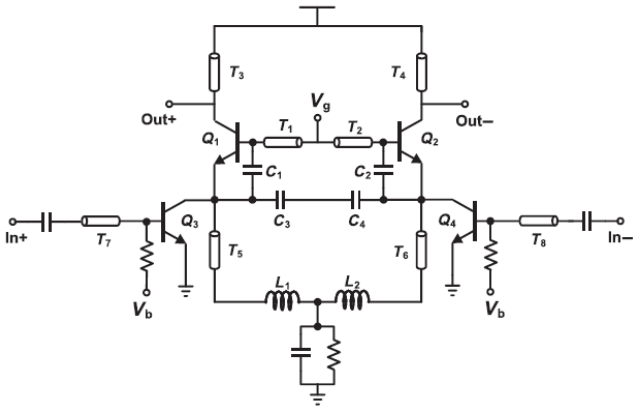


heterojunction bipolar transistors (HBTs) exhibit non-linearities in two ways: (1) inherently exponential I–V relationship and (2) distortion caused by waveform clipping when the transistor is driven into saturation by a large input swing. Plot shows the simulated collector current (Ic) and third-order derivative of Ic over Vbe versus Vbe. The term Gm3 represents the small signal transconductance of the third harmonic. From the figure, we can tell that biasing the transistor at the Class-A region (VBE > 1V) gives the highest third harmonic transconductance. However, the corresponding DC current is huge, which leads to very

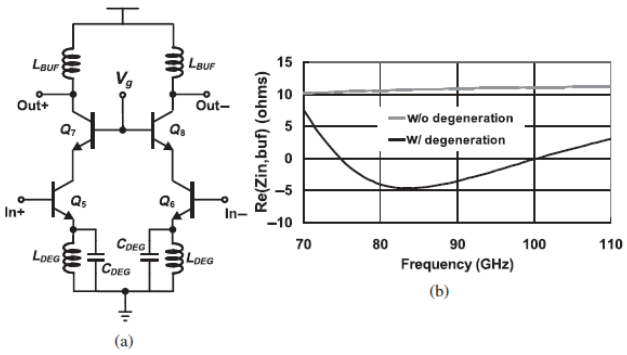
poor efficiency. On the other hand, biasing the transistor in the Class-AB regime (VBE close to 0.87V) offers good third harmonic strength with a relatively small Ic. In summary, given an input signal swing, there is an optimal bias point where the average integral in the plot is maximized.

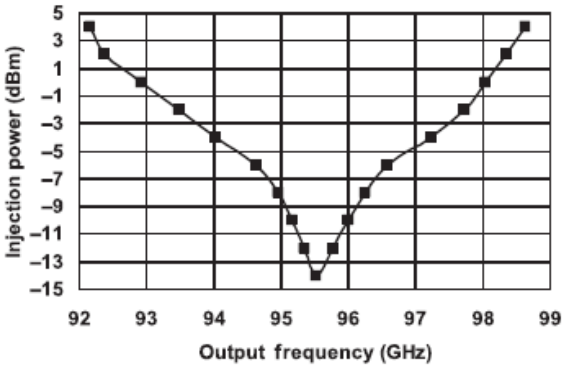


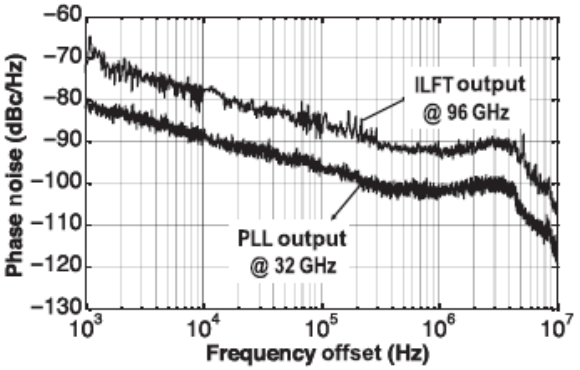
The schematic of the W-band ILFT circuit is shown above, which consists of two parts: (1) a pair of harmonic generating transistors Q3&Q4 and (2) an ILO. The harmonic generator takes advantage of the nonlinearity of the HBTs and generates all the harmonics of the input fundamental frequency, which are then injected to the ILO. The ILO is based on a differential Colpitts oscillator with a free-running frequency close to three times the input fundamental frequency, and therefore exhibits a loop gain greater than unity for the third harmonic component only. The injection-locking operation is realized by feeding the third harmonic of the input signal generated by Q3 & Q4 into the emitters of ILO. Transistors Q3 &Q4 reuse part of the DC current of the tank and are biased in the Class-AB regime for maximum third harmonic generation. The 96 GHz output signals are taken out from the collector terminals of Q1&Q2 through a cascade buffer stage to minimize leakage of the 32 GHz injection signal at the output. Differential operation is achieved by connecting two interdigitated metal-oxide-metal (MOM) capacitors (C3&C4) back-to-back across the emitters of Q1&Q2.



The input impedance seen into the base of a Colpitts oscillator is derived based on a general circuit model shown in above. The schematic of the buffer is below. The plot is the simulated the real part of buffer's input impedance with and without capacitive emitter degenration. The single-ended 96GHz output spectrum measured at the output of the ILFT is shown below. The next plot illustrates the measured input sensitivity curve of the ILFT, from which we can see that the ILFT has a free-running frequency of 95.5GHz, achieves an input sensitivity of -14dBm, and exhibits a locking range of 6.5GHz under 4dBm injection power.

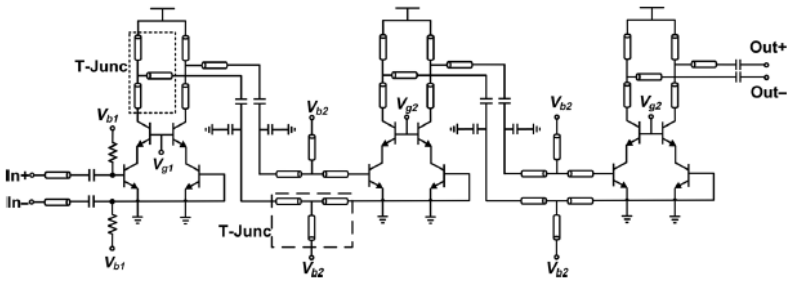




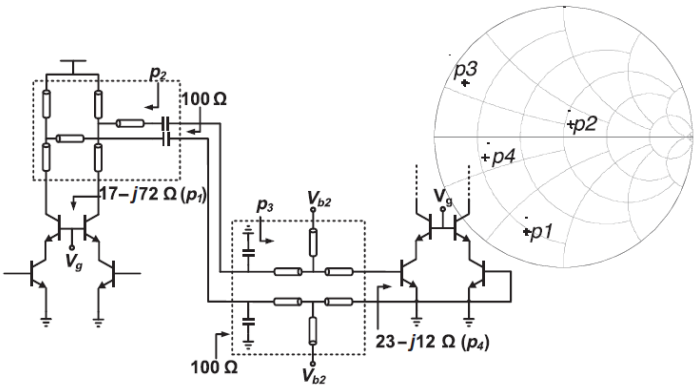


Design of a W-Band Silicon-Based HBFT

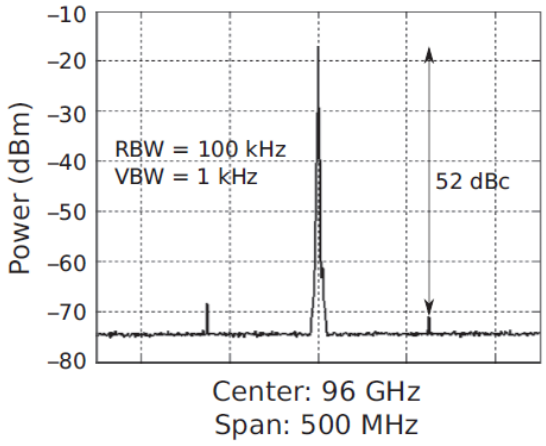
The architecture of HBFT is shown above. It consists of three stages: the harmonic generation stage, which converts a 32 GHz input signal to 96 GHz, followed by two LO amplification and filtering stages working at 96 GHz. All three



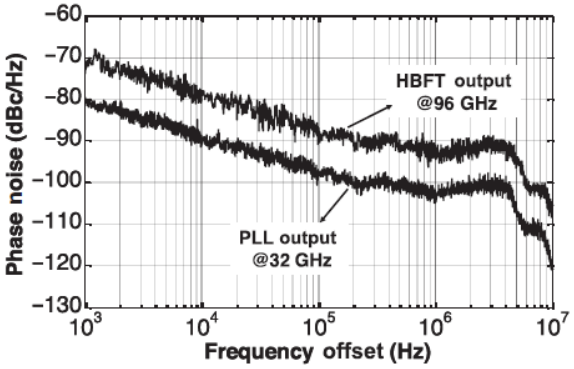
stages adopt the pseudodifferential cascode topology. Again the first stage transistor is biased at optimum third-harmonic efficiency bias voltage. In contrast, the latter two stages are biased in Class-A. In a symmetric design of a



differential amplifier the even harmonics of the collector currents are in common mode and should cancel out in the differential output voltage. The load of the amplifier is tuned to the third harmonic to maximize the gain at 96 GHz and suppress all other harmonics. The figure on the right illustrates the matching procedure on the Smith Chart.

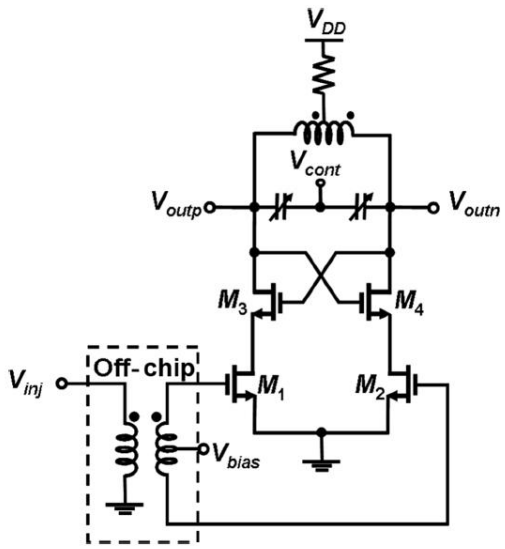


The single-ended 96 GHz output spectrum measured at the output of the HBFT is shown on the left. The tuning range measured at the output of HBFT is 90.9–101.4 GHz, which is exactly three times of the PLL tuning range, as expected. Phase noise performance was measured using a 125MHz crystal oscillator as the reference signal. The one on the right, the phase noise at 1MHz offset measured at the output of the PLL and HBFT are -103 and -92dBc/Hz, respectively. The phase noise degradation after the ILFT is 11 dB, and this value was maintained for frequency offset ranging from 1 kHz to 10 MHz. Suppression for the first and second



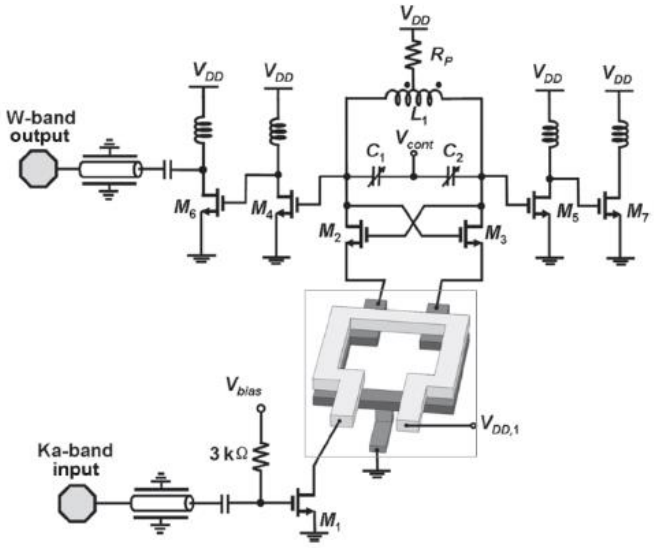
harmonics at the output of HBFT is observed to be better than 20 dB.

Design of a Transformer-Based COMS ILFT

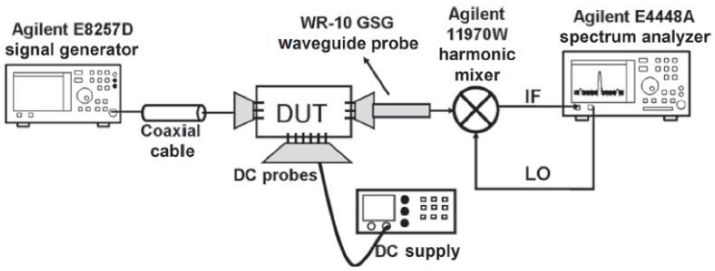


The figure on the left shows a V-band ILFT. An off-chip transformer is used to feed the input signal differentially toM1–M2 serving as harmonic generator. Because the harmonic generator shares the same current with the ILO, the gate bias of M1 and M2 (Vbias) has to be higher than Vth to maintain a sustainable oscillation for the ILO.

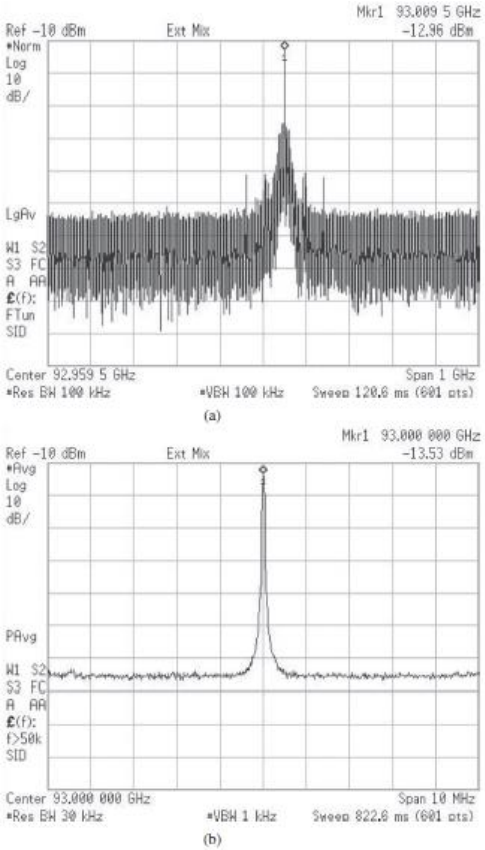
The circuit schematic of the mm-wave T-ILFT is shown below. An on-chip transformer is employed to feed the third harmonic to the ILO and, more importantly, decouple the harmonic generator from the ILO. Several benefits can be attained from the this T-ILFT structure: (1) The harmonic-generating transistor M1 can be biased independently from the ILO to achieve optimum conduction angle, while consuming negligible DC power. (2) In contrast to the circuit in Figure 10.24, the cross-coupled pair M2–M3 is not stacked on top of M1, which saves voltage headroom for the ILO. As a result, the ILO can operate at lower supply voltage with less power consumption, and larger output swing can be obtained for a given supply. (3) The transformer also converts the output impedance of M1 to a much smaller value so as to reduce the source degeneration impedance of the ILO. the T-ILFT circuit does not exhibit severe loop gain degradation, due



to the impedance transformation offered by the transformer. (4) The transformer carries out on-chip single-to-differential conversion.

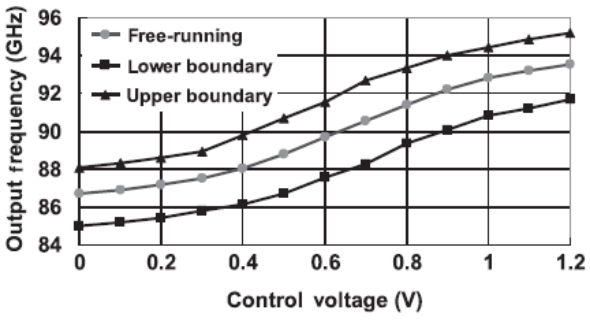


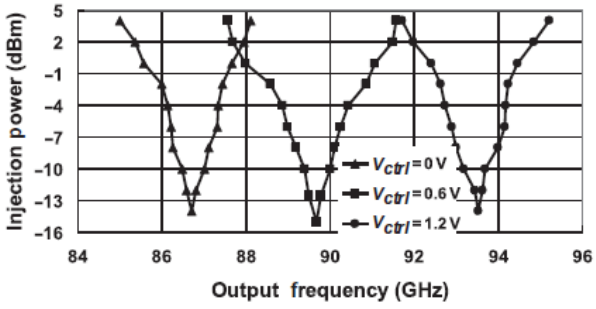
The test setup for the T-ILFT is shown on top.



The measured single-ended output spectral under free-running and injection-locked modes are shown below. The T-ILFT shows an output power of −13 dBm at 93.01 GHz under free-running, and an output power of −13.5 dBm at 93 GHz when locked to a 0 dBm 31 GHz input signal.

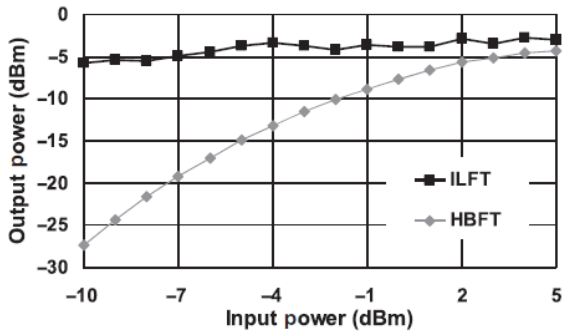
The free-running ILO achieves a measured tuning range from 86.7 to 93.5 GHz while the T-ILFT exhibits a locking range varying from 3.1 to 4.4 GHz for different control voltages, as shown on the right. By tuning the varactors, the T-ILFT covers a continuous locking range from 85 to 95.2 GHz. The figure below shows the measured input sensitivity curve of the T-ILFT under three different control voltages.





Comparisons and Discussions

Based on the measurement results of the prototypes, we now compare two kinds of SiGe frequency triplers in terms of phase noise, tuning range, and output power. The HBFT degrades the phase noise by 11 dB and triples the tuning range, i.e., it maintains the same fractional tuning range. The tuning range of the ILFT is limited by its locking range, which is highly dependent on the injection power, and the phase noise degradation is only 10 dB for the ILFT.



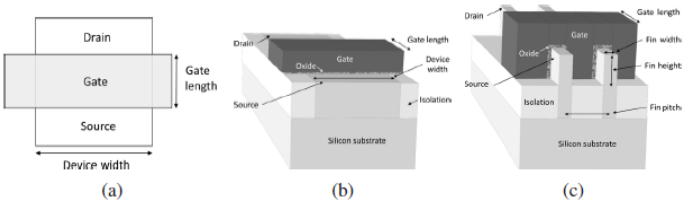
The figure on the left plots Pout vs. Pin for both HBFT and ILFT measured from the tripler breakout circuits. The ILFT's Pout is determined by the oscillation amplitude, not Pin, while the HBFT's Pout is heavily dependent on Pin. The results indicate that the ILFT is more energy efficient and is capable of providing good output power, especially when input power is low.

Two different tripler topologies (i.e., HBFT and ILFT) together with a Ka-band PLL, have been demonstrated in a 0.18 µm SiGe BiCMOS. Both chips exhibit good phase noise and harmonic suppressions and consume the same amount of power, while the main trade-off is between tuning range and output power or conversion loss.

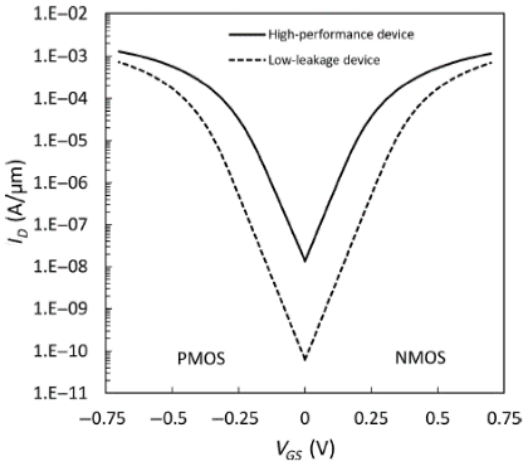
A W-band T-ILFT has been designed and implemented in 65 nm standard CMOS technology. The use of transformer enables optimum bias for the harmonic generator by decoupling it from the ILO and also reduces the source degeneration impedance of the ILO through impedance transformation. Based on the measurement results and analytical studies, the benefits of using a frequency tripler following a Ka-band PLL for W-band frequency generation were discussed and highlighted.

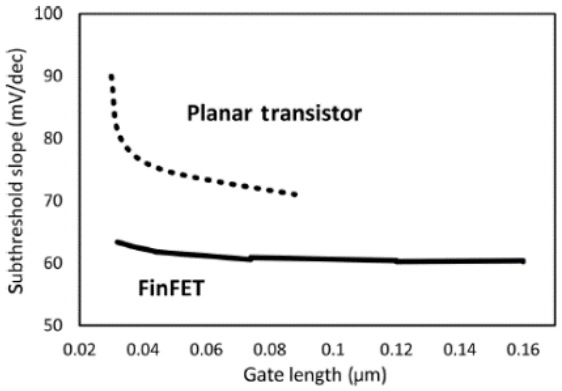
FinFET Process Technology for RF and Millimeter-Wave Applications

Overview of FinFET Technology



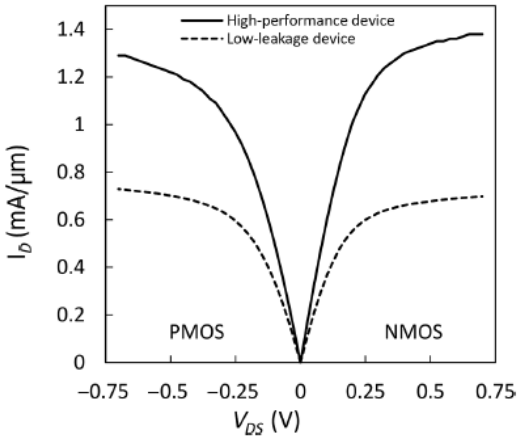
Fin field-effect transistor (FinFET) logic process technology has been widely adopted for SoC applications since its commercial introduction in 2012. In FinFET technology, traditional two-dimensional transistors are replaced by three-dimensional geometries called FinFETs. While the structure and performance of these devices are different, the layout view is identical for planar and FinFET transistors. The bottom figure shows the ID–VGS characteristics of a FinFET technology that has been optimized for RF applications. The subthreshold slope is near ideal and devices are targeted to have off currents for both N-type metal-oxide- emiconductor (NMOS) and P-type metal-oxidesemiconductor (PMOS) devices well below 100 pA/µm.





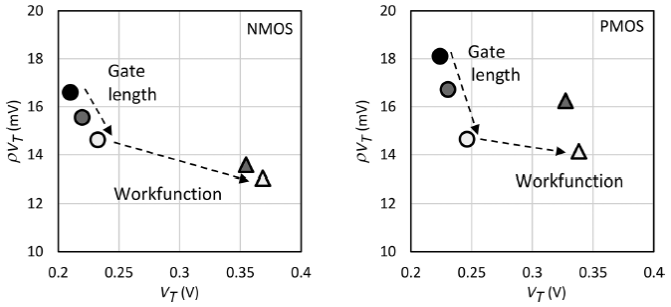
For best RF performance, devices with high drive current, low leakage, low gate capacitance, and low parasitic capacitance are paramount. To achieve this, the gate length is reduced to the point at which a sharp increase in the subthreshold slope is observed. The correlation between subthreshold slope and gate length is shown below for both planar and FinFET technologies. While at 30 nm gate

length the planar device already indicates a sharp increase, the FinFET device is still very close to the ideal subthreshold slope of 60 mV/decade. As a result, RF devices on FinFET technology are showing best performance at less than 30 nm channel length.

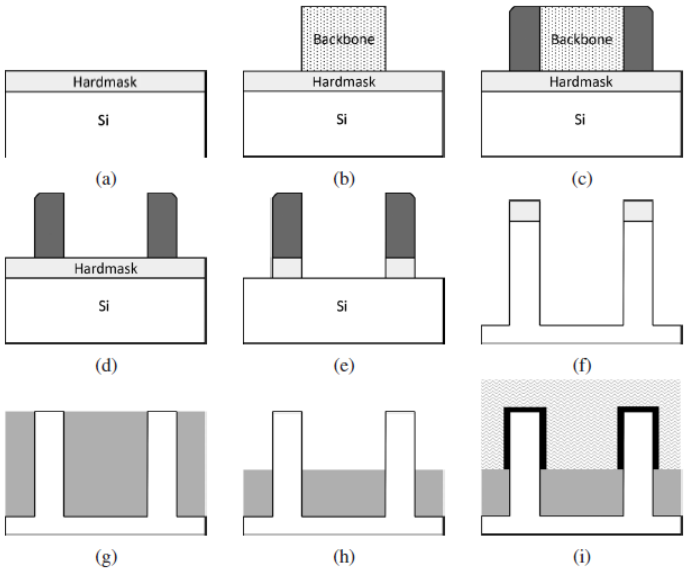


Transistor drive currents of FinFET devices are significantly higher than on any commercial planar technology. ID–VDS characteristics of an RF-optimized technology are shown on the left, demonstrating a current density greater than 13 mA/µm at 700mV supply voltage. On planar technologies, the supply voltage would need to be increased close to 1V to achieve a similar drive current. Even higher performance can be achieved when the technology is optimized for high-performance logic.

A well-targeted and optimized FinFET technology does not require any substrate doping to control short channel devices. Eliminating the substrate doping entirely and controlling the threshold voltage solely by the work function of the metal gate leads to devices with an extremely low random variation of the threshold voltage, ρVT.



The process starts with depositing a hardmask on Si and patterning a backbone material on top of this hardmask. This backbone is printed with twice the final fin pitch. This is followed by depositing and etching a spacer. The thickness of this spacer is critical, as it determines the width of the final fin. Having the fin width defined by a spacer rather than by direct printing reduces the variation of this width. In modern FinFET technologies, the width of the final fin can be controlled to within a few Angstrom. After spacer formation, the backbone



layer is removed and the pattern is transferred into the hardmask. The next step is to etch the hardmask pattern into the silicon. This forms the final fin and determines the depth of the isolation. The isolation material is deposited and polished and recessed to determine the final height of the active part of the fin. The recess step etermines the final height of the fin, and the control of this step is therefore critical to minimize performance variation. The remainder of the patterning is similar to planar technologies with the exception that the gate dielectric and the gate have to be formed on the vertical channel region.

Unique Properties of FinFET Technology for RF/mm-Wave Design Consideration

the transistor performance improvement trend has been significantly disturbed as the channel length is getting too short. The major two root causes are velocity saturation and drain induced barrier lowering (DIBL). When gate length is reduced, the drain and source start to interact more, and the gate control of the device is reduced. This effect is termed as short channel effect degradation, and the metric to measure this degradation is DIBL. FinFET technologies, however, provide excellent gate control over the thin channel by surrounding fin with three-sided gate. The lower DIBL also results in higher output resistance in the saturation mode Rout, as the drive current is insensitive to the drain voltage.

The FinFET transistor has a three-dimensional (3D) channel, called fin, wrapped around by gate material. By the nature of the 3D structure, the gate resistance has two major components, horizontal and vertical resistance.

For FinFET transistors, heat degrades performance even more as the heat is trapped within the fin structures because the fin has only a narrow thermal conducting channel, called sub-fin, to the substrate.

Assessment of FinFET Technology for RF/mm-Wave

The recent silicon evidence suggests the peak Ft of FinFET is as high as 20% below that of planar. However, the FinFET has improved its peak Fmax performance over the planar thanks to the vertical portion of gate resistance, which reduces total gate resistance up to a certain number of fins.

To achieve overall better noise performance, lowering NFmin and Gn (or increasing Rn in the impedance form) will achieve the lower total noise factor. The unity gain frequency ωt of FinFET exceeds planar at the lower bias condition by a significant amount (>50%). Therefore, one can expect a significant improvement of the thermal noise for the gain at the lower current bias condition.

The mismatch between Zin* and Zopt defines how much noise performance degradation

there is when the input matching network is designed for minimum signal reflection and vice versa. The optimum noise matching point Zopt and the input impedance Zin get closer as they frequency goes higher. They are almost conjugate, and therefore no significant effort is required in designing an input matching network.

Design Methodology for RF/mm-Wave Performance Optimization with FinFET

Wireless system design often aims for two primary performance targets: noise and linearity. In general, the silicon area of the wireless system is highly dominated by passive components, such as an embedded coil, and the coil technology is highly independent of process nodes. Also, transistor node scaling does not always bring positive impact to silicon area scaling. This is due to design rule complications and excessive parasitics in the device and metal interface within such a crowded

accessible space. Therefore, the total radio frequency integrated circuit (RFIC) power dissipation is the premier differentiator to competitor products in the market.

the noise figure is more sensitive to the matching condition. one can obtain a maximum stable gain (MSG) if there is only forward gain in the lossless network. In order to guide the low-power design at mm-wave frequency, one needs to observe the Mason gain the effectiveness of current usage to produce voltage-current gain in the device. The recent FinFET technology shows about 70–160% improvement of FoMGP over the latest generation of planar technology, and it implies 40–60% less power dissipation over the planar technology to achieve the same amount of gain. planar may outperform FinFET at the local optimum point, Id/gm of ~0.14 A/S, which consumes about 20–30% more current than FinFET for FinFETs' local optimum point.

Design Example for an mm-Wave Amplifier with the Proposed Design

The identification of major causes of degradation of RF critical metrics such as fin self-heating and excessive parasitic by complicated structural interaction is continuously driving the process technology improvement for RF and mm-wave applications. RF critical performance of FinFET technology is superior to planar transistors in three aspects: noise, power efficiency, and linearity.