

## Introduction:

“Quantum Tunneling” is a quantum phenomenon where a particle, like electron, “tunnels” through a very thin barrier without overcoming the energy level or breaking the barrier. Companies such as Samsung are developing microprocessors with MOSFET node as thin as 3nm. Quantum tunneling causes current leakage as the semiconductor gets thinner. It causes computational error, power waste, high temperature and stressed gates.

## Purpose/Aim:

In this research, most commonly used semiconductor materials and their performance is analyzed to solve quantum tunneling problem in thin semiconductor microprocessors.

## Methods:

Since essential testing equipment like Iddq or STM was not available, theoretical value of the minimum thickness to have 1 percent of tunneling probability was calculated with the assumption of the energy level generally used for commercial microprocessors. Thickness and lattice constants were referenced. The research proposes the probability density and the minimum thickness of each materials.

## Results:

$$T(L, E) = \frac{|\psi_{tra}(x)|^2}{|\psi_{in}(x)|^2} = \frac{1}{\cosh^2(\beta L) + (\gamma/2)2\sinh^2(\beta L)}$$
$$\approx 16 \frac{E}{U_0} \left(1 - \frac{E}{U_0}\right) e^{-2\beta L}, \beta = \sqrt{\frac{2m}{\hbar} (U_0 - E)}.$$

Average E in MOSFET = 7eV.

Gr/n-4H-SiC(0.36eV & 0.31nm):

$$probability = 16 \frac{7}{0.36*n} \left(1 - \frac{7}{0.36*n}\right)^* e^{-2\sqrt{26.254(0.36*n-7)*(0.31n)}} = 2.52 \times 10^{-11}\%,$$
$$n = 20, L = 6nm.$$

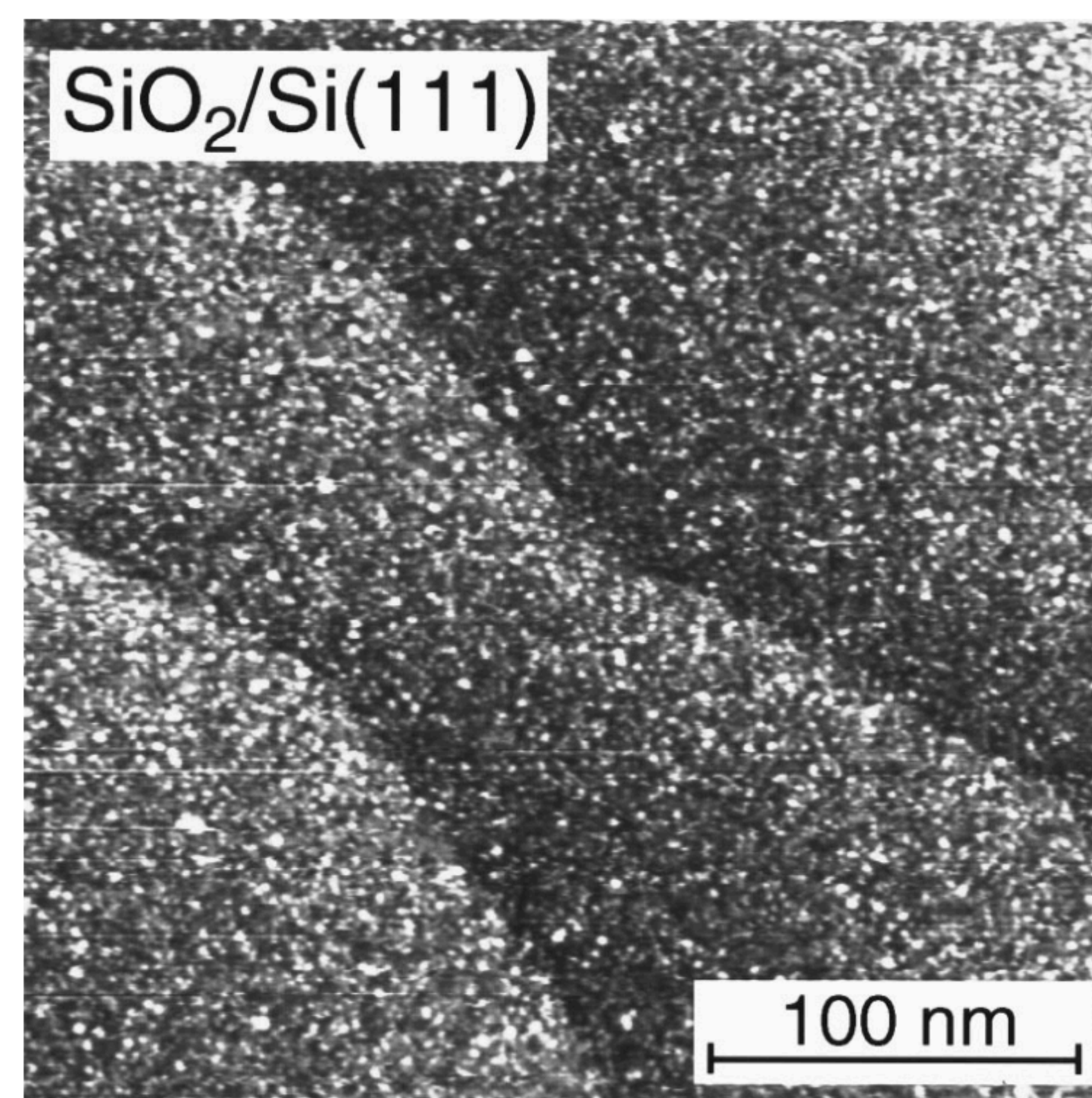
SiO<sub>2</sub>(1.1eV & 0.31nm):

$$probability = 1.10 \times 10^{-6}\%, n = 7, L = 2.17nm.$$

$\beta$  - Si<sub>3</sub>N<sub>4</sub>(5.1eV & 0.76nm):

$$probability = 2.73 \times 10^{-10}\%, n = 2, L = 1.52nm.$$

## STM image of a 1-nm-thick SiO<sub>2</sub> surface



## Discussion:

Potential barrier level is directly proportional to the number of layer of the compound, or thickness. Experimentally, it is impossible to achieve a uniform density and thickness, however, the ML(monolayer) and thickness is quantized for the ideal setting. When the potential barrier energy is lower than the electron’s energy, transmission is 1 – reflection. Ideally, insulating layers should have a transmission of 0.

## Conclusions & Future Research:

The theoretical values of three materials show that smaller the lattice constant of a semiconductor material, the thicker the tunneling threshold. In order to increase the chip density, decreasing the wafer’s layer down to atomic level is required. As an alternative, decreasing the electron energy can also be effective. In the future, replicating the research with STM and much reliable reference data of the material can produce more accurate result of the study.

## Acknowledgements:

"Properties of Silicon Carbide (SiC)". Ioffe Institute. Retrieved 2009-06-06.  
Sonde, S.; Giannazzo, F.; Raineri, V.; Yakimova, R.; Huntzinger, J.-R.; Tiberj, A.; Camassel, J. Electrical properties of the graphene/4H-SiC(0001) interface probed by scanning current spectroscopy. Phys. Rev. B 2009, 80, 241406.  
Libretexts. (2019, October 13). 7.6: Quantum Tunneling of Particles through Potential Barriers. B. El-Kareh.  
Fundamentals of Semiconductor Processing Technologies. Kluwer Academic Publishers, 1995  
Boulay, D & Ishizawa, Nobuo & Atake, T & Streltsov, V & Furuya, Kenji & Munakata, Fumio. (2004). Synchrotron X-ray and ab initio studies Of beta-Si<sub>3</sub>N<sub>4</sub>. Acta crystallographica. Section B, Structural science. 60. 388-405. 10.1107/S010876810401393X.  
Review—Silicon Nitride and Silicon Nitride-Rich Thin Film Technologies: Trends in Deposition Techniques and Related Applications Alain E. Kaloyeros, a Fernando A. Jove, b Jonathan Goff, b and Barry Arklesb